Maulana Abul Kalam Azad University of Technology, West Bengal
(Formerly West Bengal University of Technology)
Syllabus of M. Tech. (Electronics & Communication Engineering): Specialization: VLSI Design
(Effective from academic session 2021-22)

Curriculum Structure

Semester 1

Sr. No.	Course Type/Code	Course Name	Teaching Schemes			Credits
			L	T	P	
1	Core-1/MVDC101	Semiconductor Device Modelling	3	0	0	3
2	Core-2/MVDC102	Digital VLSI Design	3	0	0	3
3	Prog. Elective-1 /MVDP103	A. Processor Architecture B. Parallel Architecture and Processing C. System on Chip (SOC) Design	3	0	0	3
4	Prog. Elective-2 /MVDP104	A. CAD of Digital systems B. Fabrication Technology C. Physical Design Automation	3	0	0	3
5	Audit Course-1/MVD 105	Audit course 1	2	0	0	0
6	MVD106	Research Methodology and IPR	2	0	0	2
7	Lab-1/MVDL191	Semiconductor Device Modelling Lab	0	0	4	2
8	Lab-2/ MVDL192	Digital VLSI Design Lab	0	0	4	2
		Total	16	0	8	18

Semester 2

Sr. No.	Course Type/Code	Course Name	Teaching Schemes			Credits
			L	T	P	
1	Core-1/MVDC201	Analog VLSI Design	3	0	0	3
2	Core-2/MVDC202	Design for Testing and Verifications	3	0	0	3
3	Prog. Elective-3 /MVDP203	A. RF-VLSI Design B. Mixed Signal Circuits and Systems Design C. Memory Technology	3	0	0	3
4	Prog. Elective-4 /MVDP204	A. VLSI Signal Processing B. Digital Signal and Image Processing. C Bio Medical Signal Processing	3	0	0	3
5	Audit Course-2/MVD 205	Audit course 2	2	0	0	0
6	Lab-1/ MVDL291	Analog VLSI Design Lab	0	0	4	2
7	Lab-2/ MVDL292	Testing and Verifications Lab	0	0	4	2
8	MVD281	Mini Project	2	0	4	2
		Total	16	0	12	18

Semester 3

Sr. No.	Course Type/Code	Course Name	Teaching Schemes			Credits
			L	T	P	
1	Prog. Elective-5 /MVDP301	A. Artificial Intelligence, Machine Learning & Applications B. Selected Topics in Engineering Mathematics. C. Nano materials and nano-technology D. Low Power VLSI Design	3	0	0	3

2	Opt. Elective-1 /MVDP302	A. Business Analytics B. Industrial Safety C. Operations Research D. Cost Management of EngineeringProjects E. Composite Materials F. Waste to Energy	3	0	0	3
3	Lab-1/ MVDL391	Machine Learning using Python	0	0	4	2
4	Dissertation-I/MVDD381	Dissertation Phase – I	0	0	20	8
		Total	6	0	24	16

Semester 4

Sr. No.	**Course Type/Code**	**Course Name**	Teaching Schemes			Credits
			L	T	P	
1	Dissertation-II/ MVDD481	Dissertation Phase – II	0	0	32	16
		Total	0	0	32	16

Audit course 1 & 2

1. English for Research Paper Writing
2. Disaster Management
3. Sanskrit for Technical Knowledge
4. Value Education
5. Constitution of India
6. Pedagogy Studies
7. Stress Management by Yoga
8. Personality Development through Life Enlightenment Skills.

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MVDC101: Semiconductor Device Modelling	**Lecture/Week:3**	**Credit:3**

Course Outcomes:
At the end of this course, students will be able to

- CO1: Apply the qualitative understanding of physics of semiconductors to develop quantitative models for semiconductor phenomena relevant to the field of electronics.
- CO2: Model semiconductor homo junction and characterize p-n junction diodes
- CO3: Analyze metal semiconductor junctions and model Metal oxide semiconductorFET
- CO4: Interpret and Model Advanced semiconductor FETs like SOI FET, FinFET, TFET etc.

MODULE1:
Review: Review of quantum mechanics, Electrons in potentials (infinite barrier, potential well), Electrons in periodic lattices (KP Model), E-k diagrams, effective mass; Quasi-particles in semiconductors, electrons, holes (light holes and heavy holes), optical and acoustic phonons, electron hole pair (EHP). Band diagram of silicon.

MODULE 2:
MOS Capacitor: Energy band diagram of Metal-Oxide-Semiconductor contacts, Mode of Operations: Accumulation, Depletion, Midgap, and Inversion, 1D Electrostatics of MOS,Depletion Approximation, Accurate Solution of Poisson's Equation, CV characteristics ofMOS, LFCV and HFCV, Non-idealities in MOS, oxide fixed charges, interfacial charges,Midgap gate Electrode, Poly-Silicon contact, Electrostatics of non-uniform substrate doping, ultrathin gate-oxide and inversion layer quantization, quantum capacitance, MOS parameterextraction.

MODULE 3:
Physics of MOSFET: Drift-Diffusion Approach for IV, Gradual Channel Approximation, Sub-threshold current and slope, Body effect, Pao&Sah Model, Detail 2D effects in MOSFET, Highfield and doping dependent mobility models, High field effects and MOSFET reliability issues(SILC, TDDB, & NBTI), Leakage mechanisms in thin gate oxide, High-K-Metal Gate MOSFETdevices and technology issues, Intrinsic MOSFET capacitances and resistances, Meyer model**.**

MODULE 4:
SOI MOSFET: FDSOI and PDSOI, 1D Electrostatics of FDSOI MOS, VT definitions, Back gate coupling and body effect parameter, IV characteristics of FDSOI-FET, FDSOI-sub-threshold slope, Floating body effect, single transistor latch, ZRAM device, Bulk and SOI FET:discussions referring to the ITRS.

MODULE 5:
Nanoscale Transistors: Diffusive, Quasi Ballistic & Ballistic Transports, Ballistic planer and nanowire-FET modeling: semi-classical and quantum treatments
Advanced technologies: train Engineered Channel materials, Mobility in strained materials, Electrostatics of double gate, and Fin-FET devices High–k, TFET etc.

Text Books:

1. S.M. Sze & Kwok K. Ng, Physics of Semiconductor Devices, Wiley 2007
2. J.P. Colinge, Silicon-on-Insulator Technology: Materials to VLSI, Springer 1997
3. YannisTsividis, Operation and Modeling of the MOS Transistor, Oxford University Press 2nd Edn.

References:

4. YannisTsividis, Operation and Modeling of the MOS Transistor, Oxford University Press 2ndEdn

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MVDC102: Digital VLSI Design	**Lecture/Week:4 (3L,1T)**	**Credit:4**

Course Outcomes:

After completion of this course, students will be able to

CO1: Learn the basics of CMOS Integrated Circuit (IC), different Domains of VLSI design, design automation tools and the state-of-the-art VLSI circuits.

CO 2: Learn CMOS logic behaviour, advantages and drawbacks using static, dynamic, Domino logic and Bi-CMOS logic

CO3.Learn the basics of CMOS fabrication and Layout.

CO4: Learn EDA tools and their advantages, concept of test bench, simulation, design verification, synthesis and hardware description language (Verilog/VHDL/System 'C')

CO5: learn the concept of Programmable Hardware and their requirements, FPGA -- architecture, configuration and design flow, concept of System on Chip (SOC) .

CO6: Learn logical effort, path effort, path effort delay, path parasitic delay, designing fast circuits and multistage logic networks and the concept of delay **vs** fan out,

CO7: Learn the design of a 32-bit RISC CPU, Static RAM and Simulation, Synthesis & validation of the architectures on FPGA and analysis their performances.

MODULE 1: Introduction to VLSI Design

Basics of Integrated Circuit (IC), SSI, MSI, LSI, VLSI, ULSI, Integration levels. History of IC development, Moore's Law, Different types of IC chips; Digital, Analog & Mixed signal ICs; Different Domains of VLSI design; EDA- the VLSI design CAD tools, VLSI design state-of-the-art, some emerging applications of VLSI, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay VLSI design of complex processor, VLSI Design Flow, Synthesis, layout generation, Verification and simulation, VLSI chip manufacturing process flow.

Module2 : CMOS logic Basics

.Basics of MOS transistors and MOS as switches, Complementary CMOS logic , CMOS logic behaviour , advantages and drawbacks of CMOS logic, Pull up and pull down network, conduction complement, complex logic function using CMOS, pass transistors, transmission gates, tri-state buffers, Flip- flops(D- F/F, JK F/F etc.), transistor count, Delay , drawbacks of CMOS, Dynamic logic, Domino logic , Bi-CMOS to overcome the drawbacks of CMOS, standard cell design, full custom design. example of standard cell., combinatorial and Sequential Logic circuits –asynchronous and synchronous sequential circuits , Moore machine, Mealy machine , examples, Finite state machine design ,

Module3:Basics of CMOS Layout :

Introduction to VLSI fabrication and fabrication steps, Concept of MASK, Lithography, etching, polysilicon patterning, ion implementation , metallization etc.,fabrication error,

concept of layout , feature size, Lamda (**?**) rule, concept of process technology , stick diagram, general design rules for layout, width spacing rule, poly diffusion interaction, contacts, VIA and contact spacing, examples of CMOS layout of an inverter, NAND /NOR gates, simplified design rule, full custom and standard cell layout, placement , routing .floor planning ,

Module4: Hardware description language & EDA tools

EDA tools and their advantages, concept of test bench, simulation, , design verification , synthesis, hardware description language (HDL) -VHDL/VERILOG/SYSTEM C etc.

Module 5: Programmable Hardware and FPGA (6)
Concept of Programmable Hardware (PLA, PLD, CPLD, FPGA) and their requirements, FPGA --Architecture, configuration and design flow , system design using FPGA , concept of System on Chip(SOC). FPGA as reconfigurable computing and programmable System on Chip(pSOC). FPGA as validation of custom design or ASIC.

Module6 : Logical Effort

Logical effort -Path Logical Effort, Path Electrical Effort , Path Effort , branching effort, , delay in a logic gate, path effort delay, path parasitic delay , designing fast circuits and gate sizes, multistage logic networks, choosing the best number of stages, delay **vs** fan out,

Module7: Example of VLSI chip Design (Design of a 32-bit RISC CPU and 1K8 bit RAM

Designing a RISC CPU with fixed instruction length (32 bit) CPU, few instructions, Static RAM design with 1024 locations with each word size of 8 bits., Simulation, Synthesis & validation of the architecture on FPGA and analysis of the performance of the CPU with a small program written in machine language.

Text:

1. Carver Mead, Lynn Conway, Introduction to VLSI Systems",B.S. Publication
2. John P Uyemura ," Chip Design for Submicron VLSI",Thompson Publication.
3. Etienne Scard., Sonia Delmas Bendhia ," Advanced CMOS cell Design :",McGraw Hill Professional .
4. K.V.K.K.Prasad ,Kattula Shyamala, "VLSI Design Black Book", dreamtech Publication
5. Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation", Wiley, 2 nd Edition.

References:

1. J P Rabaey, A P Chandrakasan, B Nikolic, "Digital Integrated circuits: A design perspective", Prentice Hall electronics and VLSI series, 2 nd Edition.
2. Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation", Wiley, 2 ndEdition.
3. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits Analysis andDesign, McGraw-Hill, 1998.
4. Amitabha Sinha," Lecture Notes on VLSI Design", MAKAUT

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MVDP103 A: Processor Architecture	**Lecture/Week:3**	**Credit:3**

Course Outcomes:

At the end of this course, students will be able to

CO1. Learn the Concept of a Computer System and Design methodology of Processor Design

CO2.. Learn Datapath Design (Adder, Subtractor, multiplier etc.)

. CO3: Learn the design of hardwired control unit, microprogrammed and nano programmed Control unit.

CO4. Learn Memory Technology & design various types of memory units and memory Organization.

CO5. Learn the concept of Performance Enhancement of Processor by Pipelining and parallel Processing.

MODULE1: Concept of a Computer Systems, Basic building blocks, Store and forward concept, VonNeumann Architecture , Introduction to Processor and Processor Organisation, Introduction to Processor Architecture: Instruction Set Architecture: Instructions & Addressing, Procedures and Data, Instruction Set Variations. (2L)

MODULE2: The Arithmetic/ Logic Unit: Number Representation, Adders and Simple ALUs, Multipliers and Dividers, Floating-Point Architecture. Carry Look Ahead adders, Carry Save adder, Pipelined array multiplier, Pipelined adder .

MODULE 3: Control Unit: Hardwired control unit , Microprogram controlled unit, Nano Program Control Unit , concept of RISC and CISC Architectures, Harvard architecture , VLIW architecture.

MODULE 4: Memory Design: concept of Volatile and non-volatile memory , ROM, EPROM, EEPROM ,Static RAM, Dynamic RAM, Cache memory, Primary and secondary cache, cache cohesion, Memory System design using memory chip, Cache memory and different types of cache.

MODULE 5. Performance of a Processor**:** MIPS, MFLOPS, SPEC rating, CPI etc., Performance Enhancement of Processor by Pipelining: , Concept of Pipelining, various hazards in pipeline, methods to solve the hazards. **,**Pipelining performance measurement parameters- speedup, efficiency, throughput, design of arithmetic pipeline-,floating point adder, Multifunction pipeline, reservation table, Dynamic pipeline. Vector Processing: Characteristics of vector processing, vector instructions, Pipeline chaining, Introduction to Parallel Architecture & Processing : Flynn's classification, SIMD, MIMD machines, Interconnection Network, introduction to parallel programming Language.

Text Books:

1. J.P Hayes" Computer Architecture & Organization"(McGraw Hill)
2. Patterson & Hennessy, "Computer Organization & design, (Morgan Kaufmann)
3. Stalling ,"Computer organization and architecture, designing for performance" ,(PHI)

Reference Books:

1. Hwang, Advanced Computer Architecture ,(TMH)
2. Hwang & Briggs, "Computer Architecture & Parallel Processing", (TMH)
3. Antonakos , An Introduction to intel family of Microprocessors ,(Pearson)
4. David A. Patterson and John L. Hennessy, Computer Organization and Design ,Prentice Hall
5.Carl Hamachar, Zvonco Vranesic and Safwat Zaky ,The Hardware/Software Interface, Elsevier.
6. William Stallings, Computer Architecture and Organization, McGraw Hill.
7. A.Sinha , "Processor Architecture", (Lecture notes), MAKAUT

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MVDP103 B: Parallel Architecture and Processing	**Lecture/Week:3**	**Credit:3**

Course Outcomes:
At the end of this course, students will be able to
CO1: Identify limitations of differentarchitectures of Von-Neumann Architecture and learn different types of parallel architecture.
CO2: Learn the concept of Pipelining and different Pipelined Architecture for VLSI implementation.
CO3: Learn Super Scalar, VLIW and multithreaded Architecture.
CO4: To learn the concept of Data Flow Architecture-a non-Von Neumann architecture for performance enhancement.
CO5: Learn the concept of Programmable hardware and Reconfigurable Architecture.
CO6: Investigate issues related to Software (Parallel Programming Languages and techniques Operating Systems

Syllabus Contents:

MODULE 1: Overview of Parallel Processing, Flynn's classification, Performance analysis, Scalability, Concept of SIMD, MIMD and pipelining Architecture, Interconnection Network (Static & Dynamic), Shared Memory MIMD and distributed multiprocessor. Coarse grained and fine-grained multiprocessor

MODULE 2: Principles and implementation of Pipelining, Classification of pipelining processors, Advanced pipelining techniques, Processor level and Instruction level and Programming level pipelining, Static and Dynamic pipelining, Reservation table, Concept of Vector and Array Processing, Systolic Architecture, VLSI Array Processors.

MODULE 3: Concept of Super Scalar Architecture, VLIW processors, Case study: TI TMS 320C54X , Pentium Processor, RISC V Processor, SPARC, Intel Itanium Processor, ,
Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions.

MODULE 4: Non-Von Neuman Architecture, Concept of Data Flow Computing, Data flow diagram, Data Flow graph as Parallel Programming Language, Static and Dynamic Data Flow machines, Tagged Token Data Flow Machine, Parallel Implementation of Computational functions and "If then else "clause on Data Flow Machine, Case studies: MIT Data Flow Project, Manchester Data Flow Architecture.

MODULE 5: Programmable Hardware and Architectural concept of FPGA, FPGA Programming , Reconfigurable Computing using FPGA as basic building block, Implementation of Parallel Architecture using FPGA(s) , Case studies : Implementation of RISC Processor and Parallel Architecture for FFT algorithms on FPGA.

MODULE 6: Parallel Programming Languages,Techniques: Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues, introduction to Operating systems for Parallel Processing.

Text Books:

1.Kai Hwang, Faye A. Briggs, "Computer Architecture and Parallel Processing", MGH International Edition
2.Kai Hwang, "Advanced Computer Architecture", TMH
3.V. Rajaraman, L. Sivaram Murthy, "Parallel Computers", PHI.

4. William Stallings,"Architecture, Designing for performance"Prentice Hall, Sixth edition

References:

• H.T. Kung Kai Hwang, Zhiwei Xu, "Scalable Parallel Computing", MGH
• David Harris and Sarah Harris, "Digital Design and Computer Architecture", Morgan Kaufmann.
• Arvind, David E. Culler, "Data Flow Architecture", MIT/LCS/TM-294, 12 Feb.,1986 ,MIT,Massatusets.
• Dezso Sima, Terrence Fountain and Peter Kacsuk ," Advanced Computer Architecture" ,Pearson education,2007
• H.T .Kung ," Let's Design VLSI Algorithms", IEEE Computers, 1979
• www.ti.com
• www.xilinx.com
• Amitabha Sinha ," Lecture Notes on Parallel Architecture",MAKAUT

MVDP103C: System on Chip (SOC) Design	**Lecture/Week:3**	**Credit:3**

Course Outcomes:
At the end of this course, students will be able to
CO1: Identify and formulate a given problem in the framework of SoC based design approaches
CO2: Learn the concept of Application Specific Instructionset Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems.
CO3: Learn different simulation model, design verification and low power FPGA based Reconfigurable Systems
CO4: Develop the skill of low power SOC design with a synergy of building block optimization, power down techniques and powerconsumption verification.
CO5: Learn Role and Concept of graph theory and its relevance to circuit synthesis.
CO6: Develop skill of designing SOC with a specific case study with emphasis on area optimization, speed improvement and power minimization.

Syllabus Contents:

MODULE 1:ASIC
Overview of ASIC types, design strategies, CISC, RISC CPU Architecture and NISC approaches for SOCarchitectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.

MODULE 2: NISC
NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instructionset Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

MODULE 3: Simulation
Different simulation modes, behavioural, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable

systems, SoC related modelling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

MODULE 4: Low power SoC design / Digital system,
Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, powerconsumption verification.

MODULE 5 : Synthesis
Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trailspaths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis, Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs

MODULE 6: Case study
Case study for overview of cellular phone design with emphasis on area optimization,speed improvement and power minimization.

Text Books:

- Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge University Press, 2008.
- B. Al Hashimi, "System on chip-Next generation electronics", The IET, 2006
- RochitRajsuman, "System-on- a-chip: Design and test", Advantest America R & D Center,2000

References:

- P Mishra and N Dutt, "Processor Description Languages", Morgan Kaufmann, 2008
- Michael J. Flynn and Wayne Luk, "Computer System Design: System-on-Chip". Wiley,2011.

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MVDP104A: CAD of Digital System	**Lecture/Week:3**	**Credit:3**

Course Outcomes:
At the end of this course, students will be able to
CO1: learn VLSI design methodologies and processes.
CO2: learn the concept of VLSI design automation tools and VLSI design cycle.
CO3: VLSI Design flow and generalized methods for combinatorial optimization.
CO4: Study of various phases of CAD including simulation, synthesis, system modelling and design verification of physical design,
CO5:Demonstrate knowledge through step by step design of a simple circuit using HDL.

MODULE 1: Introduction to VLSI Methodologies – Design and Fabrication of VLSI Devices,Fabrication Process and its impact on Design.

MODULE 2: VLSI design automation tools, VLSI design Cycle: System specification, Functional design, Logic design, Circuit design, Physical design, Design verification, Fabrication, Packaging, testing, and debugging,

MODULE 3: VLSI Design Flow, general purpose methods for combinational optimization, partitioning, floor-planning, placement, routing.

MODULE 4: Simulation: pre-layout and post-layout simulation, VLSI system modelling, logic synthesis, design, verification, high level Synthesis. Detailed about lay out including standard cell layout and stick diagram.

MODULE 5: Step by step process for design and implementation of a simple circuit using HDL like VHDL/Verilog/ System "C'.

Text Books:

1. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation".
2. S.H. Gerez, "Algorithms for VLSI Design Automation.

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MVDP104B: Fabrication Technology	**Lecture/Week:3**	**Credit:3**

Course Outcomes:
At the end of this course, students will be able to

- CO1: Outline the basics of semiconductor crystal properties.
- CO2: Identify the fundamentals of IC fabrication.
- CO3: Illustrate the advanced methods involved in photolithography.
- CO4: Build an idea on process integration.

Syllabus:

MODULE 1. Introduction to VLSI technology: Device scaling and Moore's law, basic device fabrication methods, alloy junction and planar process.

MODULE 2. Crystal growth: Czochralski and Bridgman techniques, Characterization methods and wafer specifications, defects in Si and GaAs.

MODULE 3. Oxidation: Surface passivation using oxidation. Deal-Grove model, oxide characterization, types of oxidations and their kinematics, thin oxide growth models, stacking faults, oxidation systems.

MODULE 4. Diffusion and ion-implantation: Solutions of diffusion equation, diffusion systems, ion implantation technology, ion implant distributions, implantation damage and annealing, transientenhanced diffusion and rapid thermal processing.

MODULE 5. Epitaxy and thin film deposition: Thermodynamics of vapor phase growth, MOCVD, MBE,CVD, reaction rate and mass transport limited depositions, APCVD/LPVD, equipments and applications of CVD, PECVD, and PVD.

MODULE 6. Etching: Wet etching, selectivity, isotropy and etch bias, common wet etchants, orientation dependent etching effects; Introduction to plasma technology, plasma etch mechanisms, selectivity and profile control plasma etch chemistries for various films, plasma etch systems.

MODULE 7. Lithography: Optical lithography contact/proximity and projection printing, resolution and
depth of focus, resist processing methods and resolution enhancement, advanced lithography techniques for nanoscale pattering, immersion, EUV, electron, X-ray lithography.

Text Books:
1.Gandhi, S. K., "VLSI Fabrication Principles: Silicon and Gallium Arsenide", JohnWiley and Sons.
2. Sze, S.M., "VLSI Technology", 4th Ed., Tata McGraw-Hill. 1999
3. Plummer, J.D., Deal, M.D. and Griffin, P.B., "Silicon VLSI Technology: Fundamentals, Practice and Modeling", 3rd Ed., Prentice-Hall.

References:
1.Chang, C.Y. and Sze, S.M., "ULSI Technology", McGraw-Hill. 1996

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MVDP104C: Physical design automation	**Lecture/Week:3**	**Credit:3**

Course Outcomes:
At the end of this course, students will be able to

CO1: Study automation process for VLSI System design.
CO2: Understand different layout models
CO3: Understand different methods of global placement.
CO4: Learn minimization of timing-driven placement and global routing
CO5: Learn the concept of multi-layer routing.
CO6: Develop and enhance the existing algorithms and computational techniques for physicaldesign process of VLSI systems.

MODULE 1: Introduction to VLSI Physical Design Automation.
MODULE 2: Standard cell, Performance issues in circuit layout, delay models Layout styles.
MODULE 3: Discrete methods in global placement.
MODULE 4: Timing-driven placement. Global Routing Via Minimization.
MODULE 5: Over the Cell Routing - Single layer and two-layer routing, Clock and Power Routing.
MODULE 6: Compaction, algorithms, Physical Design Automation of FPGAs.

Text Books:

1. N.A. Sherwani, "VLSI Physical Design Automation"., Springer
2. S.H. Gerez, "Algorithms for VLSI Design Automation. Wiley India (pdf free download
3. S.H. Gerez , "CAD For VLSI Algorithms For VLSI Design Automation", John Wiley & sons

References:

4. Jason Cong "VLSI Physical Design Automation", Computer Science Department , http://cadlab.cs.ucla.edu/~cong/cs258f_handouts.html
5. VLSI Physical Design Automation - VAST lab at UCLA, https://cadlab.cs.ucla.edu ›

MVDL191: Semiconductor Device Modelling Lab	**Lecture/Week:4**	**Credit:2**

Course Outcomes:
At the end of this course, students will be able to

- CO1: Analyze the physics of four terminal MOS system and interpret the current voltage relation of a Metal oxide semiconductor field effect transistor.
- CO2: Model the small channel and thin oxide effects in MOSFET operation.
- CO3: Model the Characteristics of advanced FET operation.

List of Experiments:

1) MOS capacitor C-V characteristics
2) MOSFET characteristics IV and C-V, DIBL and other effects in MOSFET.
3) Carrier Transport analysis
4) Investigation of multi gated MOSFET Characteristics

Tunnel FET design and analysis

MVDL-192: Digital VLSI Lab [Sem – I] 4(P) CREDIT-2)

Teaching Scheme **Lectures : 4 hrs/week**	

Course Outcomes:

After the completion of this lab course students will be able to:
CO1 be familiarized with the steps by step process involved in VLSI design and with different EDA t (open source as well as commercial)
CO 2 write program in hardware description language (HDL) like Verilog, VHDL for digital circuits learn design verification using test bench.
CO 3 develop skill to design, simulate, synthesize and validate digital circuits on FPGA Platform usir design Tools like Xilinx ISE / Icarus Verilog.
CO 4. develop skill to design digital circuits using VLSI design Tools like DSCH & Microwind.
CO 5. Develop the skill for Layout of digital circuit using EDA tools like Cadence and Electric.

Pre-requisite: Knowledge of high-level structured programming Language (preferably 'C' and /or HDL), Digital electronics.

Software & Hardware Tools –

Sl. No	**Software Name / Hardware**	**Open Source / Purchase**
1.	Xilinx ISE with iSim Simulator	Open Source Software
2.	Icarus Verilog with GTK Wave	Open Source Software
3.	DSCH and Microwind	Open Source Software
4.	Electric with LT Spice	Open Source Software
5 6..	FPGA Kit (Hardware) Cadence EDA Software	Commercial Commercial

Part-A : FPGA Based Digital Design, synthesis and Validation

LAB – 1A: Introduction to FPGA Based Digital Design:
- Register-transfer-level abstraction
- Introduction to HDL Coding by Basic Digital Gates, Concept of Test Benches.
- Using Xilinx ISE Pack for HDL Coding, Simulation & Synthesis

LAB – 1B: Understanding the FPGA Board
- Identifying the Board Parts
- Procedure of Bit-Stream Downloading by Basic Digital Gates
- JTAG

LAB – 2: Writing HDL(Verilog, VHDL) Code, Test Bench for Simulation & Synthesis
- Combinational Circuit – Multiplexer, Demultiplexer, Decoder, Encoder, Half Adder, Full Half Subtractor, Full Subtractor, Adder- Subtractor.
- Combinational Circuit – Ripple Carry, Carry look ahead adder
- Construction of Higher Level Multiplexer using Lower Level Multiplexer
- Circuit Designing using universal logic: Multiplexer

LAB – 3: Writing HDL (Verilog, VHDL) Code, Test Bench for Simulation & Synthesis
- Sequential Circuit –
- Flip-Flop – SR, D, JK, T
- Counter – Up, Down, Bidirectional, Ring, Ripple, Johnson, Mod-N.
- Register – Left/Right Shift Register, Construction of Memory.
- FSM – Mealy & Moore

LAB – 4: Writing Verilog Code, Test Bench for Simulation & Synthesis
1. ALU Design 2. A 12-bit CPU Design 3.FFT Processor Design

Part-B : Lab assignments with VLSI Design Automation tool (Cadence , DSCH and Microwind) for Layout Design.

LAB – 5: Lab assignments with Cadence , DSCH , Microwind:

- Familiar with VLSI Design Tools like: **Cadence, DSCH , Microwind**.
- Study and Validation of the behavior of the basic logic Gates on DSCH schematic windo Extract their layouts using Microwind.
- Study and Validation of the behavior of Combinational logics a) Full adder using half adder subtractor using half subtractor c) Binary adder sub tractor circuit and d) Ripple carry adder on DSCH schematic window and Extract the layout using Microwind.

LAB – 6: Lab assignments with Cadence and Micro wind:

- Study and Validation of the behavior of a) Parity checker circuit, b) 2:4 decoder circuit, c) mux using 2:1 mux circuit and d) 1 bit comparator circuit on DSCH schematic window and the layout using Microwind.
- Study and Validation of the behavior of 2:1 mux as a universal logic on DSCH schematic v and Extract their layouts using Microwind.

LAB – 7: Lab assignments with DSCH and Microwind:

- Study and Validation of the behavior of Sequential logics a) Flip-flops: S-R, D, J-K, T b)Reg Counter: Ripple, Ring, Up, Down, Mod-N Counter circuit on DSCH schematic window and the layout using Microwind.

LAB – 8: Lab assignments with DSCH and Microwind:

- Study and Validation of the behavior of a) CMOS inverter circuit and b) CMOS- NOR ci CMOS XOR circuit and d)CMOS Combinational circuit on DSCH schematic window and the layout using Microwind.

Part-C : Lab assignments with Cadence, Electric

LAB – 9: Lab Assignments with Cadence, Electric:

- Familiar with Schematic design and test using Electric.
- Study and Validation of the behavior of the basic Gates on Electric schematic window and their layouts using Electric.
- Study and Validation of combinational logic such as a) full adder using half adder, b) Full sub circuit, c) Ripple carry adder circuit, d) Binary adder subtractor circuit and e) Parity checker and Extract the layout using Cadence, Electric.

LAB – 10: Lab Assignments with Cadence, Electric:

- Study and Validation of a) 2:4 decoder circuit and b) 4:1 mux using 2:1 mux circuit, c comparator circuit and Extract the layout using electric.
- Study and Validation of the behavior of 2:1 mux as a universal logic and extract the layou Cadence, Electric.

LAB – 11: Lab Assignments with Cadence, Electric:

- Study and Validation of Sequential logics a) Flip-flops: S-R, D, J-K, T b)Register c) Coun Extract the layout using electric
- Learn to design and Test of a) CMOS inverter b) CMOS-NAND, c) CMOS-XOR and Combinational circuit and Extract the layout using Cadence, Electric.

Text Books:

1. Advanced Digital Design using Verilog-HDL , Michael. D. Ciletti, PHI publications.
2.Carver Mead, Lynn Conway, Introduction to VLSI Systems",B.S. Publication
3.John P Uyemura ," Chip Design for Submicron VLSI",Thompson Publication.
4. Etienne Scard., Sonia Delmas Bendhia ," Advanced CMOS cell Design :",McGraw Hill Professional .

References:

1.K.V.K.K.Prasad ,Kattula Shyamala, "VLSI Design Black Book", dreamtech Publication
2.Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation", Wiley, 2nd Edition1.
3.Amitabha Sinha, "Lecture Notes on VLSI Design ", MAKAUT

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Semester 2
Detailed Syllabus

MVDC201: Analog VLSI Design	**Lecture/Week:3**	**Credit:3**

Course Outcomes:
At the end of this course, students will be able to

- CO1: Model various components in CMOS process to estimate their performance in circuits.
- CO2: learn the concept of single and multistage amplifiers and biasing circuits for different CMOS amplifiers.
- CO3: Frequency response and statistical noise analysis of different single stage, multistage and feedback amplifiers
- CO4: learn design and analysis including gain -bandwidth, noise and stability of Operational Amplifiers and CMOS design of high-performance Op-amps.
- CO5: learn the concept of flexible and discrete analog circuits i.e., Switched Capacitor circuits and will also be familiarized with Field Programmable analog Circuit

Syllabus Contents:

MODULE 1: CMOS device fundamentals: Basic MOS models, device capacitances, parasitic resistances, substrate models, transconductance, output impedence, frequency dependence of device parameters, performance analysis.

MODULE 2: Single stage amplifiers: Common source amplifier, source degeneration, source follower, common gate amplifier, cascade stage.
Differential Amplifiers: Basic differential pair, common mode response, differential pair with MOS loads, Gilbert Cell, device mismatch effects, input offset voltage.
Current Mirrors, Current and Voltage Reference: Basic current mirrors, cascade current mirrors, active current mirrors, low current biasing, supply insensitive biasing, temperature insensitive biasing, impact of device mismatch.

MODULE 3: Frequency Response of Amplifiers: Miller effect, CS amplifier, source follower, CG amplifier, cascade stage, differential amplifier, Multistage amplifier.
Feedback: Feedback topologies, effect of load, modeling input and output ports in feedback circuits Noise: Statistical characteristics, types of noise, single stage amplifiers, differential pair, noise bandwidth, impact of feedback on noise.

MODULE 4: Operational Amplifiers: Performance parameters, One-stage and two-stage Op Amps, gain boosting, comparison, common mode feedback, input range, slew rate, power supply rejection, noise in Op Amps Stability and Frequency Compensation: Multi pole systems, phase margin, frequency compensation, High performance CMOS Op-amps: High speed/frequency

Op-amps,Differential output op-amps, low noise and low voltage op-amps.

MODULE 6: concept of flexible Analog circuits, switched capacitor and discrete Analog circuits, Discrete domain frequency analysis and transfer functions of switched capacitor circuits, switched capacitor-based filter design, concept of mixed signal circuits and architecture and operation of Field Programmable Analog Array (FPAA), Design of adders/subtractors, multipliers, differentiator and integrator using FPAAs.

Text Bookss:

1. Razavi, B., "Design of Analog CMOS Integrated Circuits", 1st Ed., McGraw Hill.2001
2. Gray, P.R., Hurst, P. J., Lewis, S.H., Meyer, R.G., "Analysis and Design of Analog Integrated Circuits", 4th Ed., John Wiley and Sons. 2001
3. Baker, R. J., Li, H. W. and Boyce, D. E., "CMOS Circuit Design, Layout and Simulation", Prentice-Hall of India. 1998

References:

4.Sedra & Smith, "Microelectronic Circuits: Theory and Applications" The Oxford series in Electrical & Computer Engineering, Seventh Edition.
5.Ramon Pallas-Areny, John G.Webster, " Analog Signal Processing",Willey Student Edition.
6. AN231E04 Datasheet Rev 1.3
7. A Programmable and Configurable Mixed-Mode FPAA SoC, Jennifer Hasler et al., Georgia Tech., January 7, 2016". doi:10.1109/TVLSI.2015.2504119.
8. RECENT TRENDS IN FPAA DEVICES V. ILA, J. BATLLE, X. CUFI, R. GARCIA Institute of Informatics and Applications from University of Girona Campus Montilivi, edifici PIV, 17071 Girona, Catalunya, Spain.
9. David Johns and Ken Martin, "Switched -Capacitor Circuits", Lecture notes :University of Toronto, (johns@eecg.toronto.edu)/ (martin@eecg.toronto.edu).
10Amitabha Sinha, "Lecture Notes on Switched Capacitor", MAKAUT

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MVDC202: VLSI Design Verification and Testing	**Lecture/Week:3**	**Credit:3**

Course Outcomes:
At the end of this course, students will be able to
CO1: Familiarity of Frontend design and verification techniques, automatic testing equipment and create reusable testenvironments.
CO2: Learn various EDA tools for testing, verification guidelines and processes.
CO3: Verify increasingly complex designs more efficiently and systematically through different Procedural statements and routines.
CO4: Acquire the concept of Randomization in System Verilog, Constraint details and the pre-randomize and post-randomize functions,
CO5: To acquire the concept of Automatic Test pattern Generation (ATPG), Fault coverage, different Fault models, Fault Simulation and Analysis.
CO6: To understand the concept of boundary scan technique and acquire the skill of debugging digital, analog and mix signal VLSI circuits using JTAG.

Syllabus Contents:

Module 1: Basic concept of Testing & Verification and their differences, Automatic Testing equipment., testing in different stages of manufacturing, Design verification, chip yield, system level operation and testing, different testing algorithms,

Module 2: EDA tools for testing, Verification guidelines: Verification Process, Basic Testbench functionality, directed testing, Methodology basics, Constrained-Random stimulus, Functional coverage, Testbenchcomponents, Layered testbench, Building layered testbench, Simulation environment phases, Maximum code reuse, Testbench performance.

. **Module 3:** Procedural statements and routines: tasks, functions and void functions, Routine arguments, returning from a routine, Local data storage, Time values Connecting the testbench and design: Separating the testbench and design, Interface constructs, Stimulustiming, Interface driving and sampling, Connecting it all together, Top-level scope Program – Module interactions.

Module4: Randomization, what to randomize, Randomization in System Verilog,Constraint details solution probabilities, controlling multiple constraint blocks, Valid constraints, In-line constraints, The pre-randomize and post-randomize functions,

Module 5:. Concept of Automatic Test pattern Generation (ATPG), Fault coverage, Fault models, Stuck-at -1, stuck-at-0 faults, transistor faults, collapsed faults, bridging faults, Delay Faults and Crosstalk, pattern sensitivity and coupling faults. Automatic Test Pattern Generation (ATPG): Algorithms for generating sequence of test vectors for a given circuit based on specific fault models, Fault analysis and Simulation to emulate fault models in CUT and application of test vectors to determine fault coverage: Parallel, deductive, and concurrent fault simulation, Design for testability, Scan, Built in self test ,Pseudo random number generator, Automatic Test Generation, Built in Logic Block observer (BILBO).

Module 6: Boundary Scan , JTAG (IEEE standard 1149.1) concept , Architecture and Instruction set and Boundary Scan TAP control operation ,testing process using JTAG(IEEE1149.4) for testing of Analog and Mixed signal VLSI circuits, Differences from digital testing , Test procedures, DSP based mixed signal test, Test plan , Boundary Scan Architecture & instruction Set of Mixed Signal Testing (IEEE1149.4) and test Process , Standard Analog Test Bus (ATB), Basic Mixed Signal Chip structure IEEE 1149. , Digital /Analog Interfaces ,Analog test access Port, Test Bus Interface circuit (TBIC), TBIC Switching Patterns, Chaining of 1149.4 compliance ICs.

Text Books:

1. N. K. Jha et.al.,"Testing of Digital Systems"
2. M L Bushnell and V D Agrawal. , "Essentials of Electronic Testing"
3. M Abramovici and A D Friedman. , " Digital Systems Testing and Testable Design"
4..M. L. Bushnell and V.D. Agrawal, Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits, Springer, 2005.
5. M. Abramovici, M. Breuer, and A. Friedman*, Digital System Testing and Testable Design*, IEEE Press, 1994

References:

1.Chris Spears, " System Verilog for Verification", Springer, 2nd Edition
2.M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers
3.IEEE 1800-2009 standard (IEEE Standard for System Verilog— Unified Hardware Design Specification, and Verification Language).
4. Amitabha Sinha, "Lecture notes on Testing & Verification of VLSI circuits", MAKAUT.
5. H. Fujiwara, *Logic Testing and Design for Testability*, MIT Press, 1985
6. T. Kropf, Introduction to Formal Hardware Verification, Springer Verlag, 2000

MVDP203A: RF VLSI Design	**Lecture/Week:3**	**Credit:3**

Course Outcomes:
At the end of this course, students will be able to
CO1: Adapt to venture deep into the RF spectrum
CO2: Relate to the inventory of RF device models
CO3: Demonstrate an understanding of the language, basic operation and design of basic RF modules
CO4: Apply the understanding to the design of wireless systems and other allied fields appreciating thetrade-offs between noise, linearity, spectral cost etc.

Syllabus Contents:

Module 1:
Basics of RF circuit design - Noise: Available noise power, noise figure Linearity & distortion: Third-order intercept point, second-order intercept point, 1-dB compression point, broadband measures of linearity - Modeling of active & passive components at high frequencies Impedance matching: broadband matching, power matching & noise matching High frequency amplifiers: bandwidth estimation using open-circuit & short-circuit time constants - using
zeros to enhance bandwidth - shunt-series amplifiers, tuned amplifiers & cascaded amplifiers

Module 2:
RF power amplifiers: Design of class A, AB, B, C, D, E, F, G & H amplifiers - Low-noise amplifier (LNA). CS, CG & cascode amplifiers, shunt-series feedback amplifiers, noise & linearity of amplifiers, amplifiers using differential configurations, Low voltage topologies for LNA, DC bias networks for LNA, design of broadband LNA
Mixers: Mixing operation, mixing with nonlinearity, mixer noise & linearity, mixer with local oscillator switching, popular mixer configurations like the Moore mixer, mixer with simultaneous noise and power match, mixer employing current reuse for low power applications

Module 3:
Oscillators: Negative resistance-based LC resonator, Colpitts oscillator, differential topologies, phase noise in oscillators, tunable oscillators Phase-locked loops (PLL) & frequency synthesizers, PLL components, continuous-time and transient behavior of PLL, in-band and out of-band phase noise Frequency synthesizers: Integer-N & fractional-N synthesizers, spurious components in synthesizers.

References:
1. John W M Rogers & Calvin Plett, “Radio Frequency Integrated Circuit Design”, 2nd Edition,Artech House, 2010
2. Richard Chi-Hsi Li,” RF Circuit Design”, John Wiley & Sons, 2009
3. Hooman Darabi, “Radio Frequency Integrated Circuits & Systems”, Cambridge UniversityPress, 2015
4. Behzad Razavi, “RF Microelectronics”, 2nd Edition, Prentice Hall, 2012
5.Thomas H Lee, “The Design of CMOS Radio-Frequency Integrated Circuits”, 2nd Edition, Cambridge University Press, 2004

MVDP203B: Mixed Signal Circuits and Systems	**Lecture/Week:3**	**Credit:3**

Course Outcomes:
At the end of this course, students will be able to

- Learn Switched Capacitor based flexible Discrete Analog Circuit like FPAA and Mixed Signal Circuits like DAC, ADC, PLL etc.
- Acquire skill on filter design in mixed signal /discrete Analog mode.
- Acquire skill on designing different architectures in mixed signal mode.

UNIT -1: Concept of Mixed Signal Circuits and examples, Need of Mixed Signal Circuits, Concept of Flexible Analog circuits, Switched Capacitor (SC) Circuits as flexible Analog circuits and concepts , SC circuit as Programmable Resister, basic elements of SCs , Operation and Analysis, Nonideal effects in SC circuits, SC based integrators ,differentiators, Adders , Subtractors, constant coefficient Multiplier and Delay Unit (Z^{-1}).

UNIT 2: Concept of Sampling, Nyquist sampling theorem and conversion of Continuous Analog to Discrete Analog Signals, Synchronous Sampling, Programmable sampling circuits, Discrete-analog Signal Processing using SC circuits, Discrete mixed signal Analog Filter Design, Programmable Analog circuit using SC as building blocks, FPAA as flexible mixed signal circuit: Concept of FPAA, advantages and drawbacks, FPAA architecture ,Programming an FPAA

UNIT 3: Analog Signal Switching, Multiplexing and Sampling, introduction to signal acquisition, ideal Analog Switch, errors in analog Switches, Analog Multiplexers, , Switching and Control models for Analog Multiplexers, AC/DC models and errors in Analog Multiplexers, Cross point Switch arrays, sample and hold circuit .

UNIT 4: Concept of Analog to Digital Signal Conversion using ADC, DC and dynamic specifications, Sampling error, Quantization noise, Different ADCs: Successive approximation, Flash, Pipelined, Sigma Delta, Hybrid converters etc., Digital to Analog conversion, error in Digital to Analog conversion.

UNIT 5: Phased Lock Loop (PLL): Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non- ideal effects in PLLs, PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.

UNIT 6 : Impedance transformation and conversion , AC/DC Signal conversion , Analog Signal rectification ,Peak and Valley detection, Direct Computation RMS to DC conversion, Implicit computation RMS to DC conversion, Analog Multiplier and Divider circuits: Transconductance Multipliers, Log- Antilog Multiplier/Divider , Amplitude Demodulation, Envelope detection, Coherent Demodulation, Two phase reference Coherent Demodulation, ,.

Text Books:

- R. Jacob Baker, "CMOS Mixed-Signal Circuit Design",Wiley Interscience, 2009.
- Ramon Pallas -Areny, John G.Webster, " Analog Signal Processing",Willey India,2012
- Behzad Razavi,"Design of Analog CMOS Integrated Circuits", TMH Edition, 2002

References:

- Philip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design" ,OxfordUniversity Press, International Second Edition/Indian Edition, 2010.
- David A. Johns,Ken Martin, "Analog Integrated Circuit Design", Wiley StudentEdition, 2013.
- -Rudy Van DePlassche, "CMOS Integrated Analog-to- Digital and Digital-to-Analog converters" Kluwer Academic Publishers, 2003
- Richard Schreier, "Understanding Delta-Sigma Data converters", Wiley Interscience,2005.

MVDP203C: Memory Technologies	**Lecture/Week:3**	**Credit:3**

Course Outcomes:
At the end of this course, students will be able to

- Select architecture and design semiconductor memory circuits and subsystems.
- Identify various fault models, modes and mechanisms in semiconductor memories and their testing procedures.
- Knowhow of the state-of-the-art memory chip design

Syllabus Contents:

Unit 1: Random Access Memory Technologies:
Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS
SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific
SRAMs.

Unit 2:DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and
Architecture, Application Specific DRAMs.SRAM and DRAM Memory controllers.

Unit 3: Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate
EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

Unit 4: Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure
Modes and Mechanism, Nonvolatile Memory, Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing.

Unit 5 : Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Floating Gate Analog memory, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices.

Unit 6: Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging

References:

- Ashok K Sharma, "Advanced Semiconductor Memories: Architectures, Designs and Applications", Wiley Interscience
- Kiyoo Itoh, "VLSI memory chip design", Springer International Edition
- Ashok K Sharma," Semiconductor Memories: Technology, Testing and Reliability , PHI

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MVDP204A: VLSI Signal Processing	**Lecture/Week:3**	**Credit:3**

Course Outcomes:
At the end of this course, students will be able to
CO1: acquire knowledge about DSP algorithms, its DFG representation, pipelining and parallel processing approaches.
CO2: acquire knowledge about retiming techniques, folding and registerminimization path problems.
CO3: Ability to have knowledge about algorithmic strength reduction techniques and parallel processing of FIR and IIR digital filters.
CO4: acquire knowledge about finite word-length effects and round off noise computation in DSP systems.

Syllabus Contents:

Module 1:Introduction to DSP systems, Pipelined and parallel processing.
Module 2:Iteration Bound, Retiming, unfolding, algorithmic strength reduction in filters and Transforms.
Module 3:Systolic architecture design, fast convolution, pipelined and parallel recursive and adaptive filters, Scaling and round off noise.
Module 4: Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic.
Module 5:Numerical strength reduction, synchronous, wave and asynchronous pipe lines, low power design.
Module 6:Programmable digital signal processors.

Text Books:

1.Keshab K. Parthi[A1], VLSI Digital signal processing systems, design and implementation [A2] , Wiley, Inter Science, 1999.
2.Mohammad Isamail and Terri Fiez ,"Analog VLSI signal and information processing", McGraw Hill, 1994
3.S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, Prentice Hall, 1985.

References:

4. www.cs.berkeley.edu/~pattrsn/152F97/slides/CS152_dsp.pdf
5. Bob Brodersen, "Introduction to Architectures for Digital Signal Processing" (http://infopad.eecs.berkeley.edu)
6. Mike Schulte," Application-Specific Processor Design", http://www.eecs.lehigh.edu/~mschulte/ece450-00
7.Uwe Meyer-Baese ," Digital Signal Processing with Field Programmable Gate Arrays", Springer, third edition.
8. www.ti.com , www.analog.com, www.xilinx.com

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MVDP204B: Digital Signal and Image Processing.	**Lecture/Week:3**	**Credit:3**

Teaching Scheme

Lectures: 3 hrs/week

Course Outcomes:

At the end of this course, students will be able to

CO1: Analyze discrete-time signals and systems in various domains

CO2: Design and implement Digital Filters (FIR, IIR) using fixed and floating point Arithmetic on targeted platforms.

CO3: learn various transform algorithms for image coding and compression.

CO4: Will be able to design, implement, compare and analyze computational complexities of different color Image Processing algorithms and to handle challenges.

CO5: learn architecture of different DSP Processors (16 bit/32-bit processors from TI, analog Devices) and VLSI architectures for implementation of Signal and Image Processing algorithms

Syllabus Contents:

MODULE 1: Review of Discrete Time signals and systems, Characterization in time and frequency, Z transform, Fourier Transform: Discrete time FT, DFT, FFT algorithms – In place computations, Butterfly computations, bit reversal technique.

MODULE 2: Digital Filter design: FIR - Windowing and Frequency Sampling, IIR– Impulse invariance, bilinear transformation, fixed and floating-point implementation, challenges and techniques.

MODULE 3: Digital Image Acquisition, Enhancement, Restoration. Digital Image Coding and Compression – Cosine Transform, Wavelet Transform, JPEG and JPEG 2000.

MODULE 4: Detailed about Color Image processing – Handling multiple planes, computational challenges, different algorithms and detailed analysis of computational complexities .

MODULE 5: Hardware Platforms for implementing signal Processing Algorithms: DSP Processors (16 bit/32 bit from TI, analog Devices) , FPGAs and VLSI architectures for implementation of Signal and Image Processing algorithms, Pipelining , SIMD and Systolic architecture

Text Books:

1. J.G. Proakis, Manolakis "Digital Signal Processing", Pearson, 4 th Edition
2. Gonzalez and Woods, "Digital Image Processing", PHI, 3 rd Edition
3. S. K. Mitra. "Digital Signal Processing – A Computer based Approach", TMH, 3 rd Edition, 2006
4. A. K. Jain, "Fundamentals of Digital Image Processing", Prentice Hall
5. Munesh Trivedi, Digital Image Processing, Khanna Publishing House.

References:

1.KeshabParhi, "VLSI Digital Signal Processing Systems – Design and Implementation", Wiley India

2.Theory and Problems of Digital Signal Processing- M.H. Hayes (Tata Mcgraw- Hill

Publishing Co.)
3.. Digital Signal Processing- Steve White (Cengage Learning,India edition)
4.Chassing, Donald Reay,".Digital Signal Processing & Applications with the TMS320C6713 and TMS320C6416" ,DSK – R. (Willey student edition)
5. www.ti.com , www.analogdevices.com , www.xilinx.com
6.. Amitabha Sinha," Lecture notes on Digital Signal Processing" ,MAKAUT
7. S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, Prentice Hall, 1985.
8. www.cs.berkeley.edu/~pattrsn/152F97/slides/CS152_dsp.pdf
9.. Bob Brodersen, "Introduction to Architectures for Digital Signal Processing" (http://infopad.eecs.berkeley.edu)
10. Mike Schulte," Application-Specific Processor Design", http://www.eecs.lehigh.edu/~mschulte/ece450-00
11.Uwe Meyer-Baese ," Digital Signal Processing with Field Programmable Gate Arrays", Springer, third edition

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MVDP204C: Biomedical Signal Processing.	**Lecture/Week:3**	**Credit:3**

Course Outcomes:
At the end of this course, students will be able to

- Understand different types of biomedical signal.
- Identify and analyze different biomedical signals.
- Find applications related to biomedical signal processing

Module 1:
Acquisition, Generation of Bio-signals, Origin of bio-signals, Types of bio-signals, Study of diagnostically significant bio-signal parameters
Module 2:
Electrodes for bio-physiological sensing and conditioning, Electrode-electrolyte interface, polarization, electrode skin interface and motion artefact, biomaterial used for electrode, Types of electrodes (body surface, internal, array of electrodes,microelectrodes), Practical aspects of using electrodes, Acquisition of bio-signals (signal conditioning) and Signal conversion (ADC's DAC's) Processing, Digital filtering
Module 3:
Biomedical signal processing by Fourier analysis, Biomedical signal processing by wavelet (time-frequency) analysis, Analysis (Computation of signal parameters that are diagnosticallysignificant)
Module 4:
Classification of signals and noise, Spectral analysis of deterministic, stationary random signals and non-stationary signals, Coherent treatment of various biomedical signal processing methods and applications.
Module 5:
Principal component analysis, Correlation and regression, Analysis of chaotic signals Application areas of Bio–Signals analysis Multiresolution analysis(MRA) and wavelets, Principal component analysis(PCA), Independent component analysis(ICA)
Module 6:
Pattern classification–supervised and unsupervised classification, Neural networks, Support vector Machines, Hidden Markov models. Examples of biomedical signal classification examples.

References:

1. W. J. Tompkins, "Biomedical Digital Signal Processing", Prentice Hall, 1993.
2. Eugene N Bruce, "Biomedical Signal Processing and Signal Modeling", John Wiley & Son's publication, 2001.
3. Myer Kutz, "Biomedical Engineering and Design Handbook, Volume I", McGraw Hill, 2009.
4. D C Reddy, "Biomedical Signal Processing", McGraw Hill, 2005.
5. Katarzyn J. Blinowska, JaroslawZygierewicz, "Practical Biomedical Signal Analysis Using MATLAB", 1st Edition, CRC Press, 2011.

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MVDL291: Analog VLSI DesignLab	Lecture/Week:4	Credit:2

Course Outcomes:
After the completion of the course , students will be able to

CO1. be familiarized with VLSI Tool like cadence virtuoso.
CO2. design analog circuit using schematic editor window and also be able to test the design.
CO3. extract the Layout of analog circuits and CMOS circuits using Layout-XL.
CO4. Carry on transient, dc and ac analysis of the designed circuit using cadence virtuoso.
CO5. understand the DRC check, LVS and RC Extraction.
CO6. be familiarized with LTSpice Tool and design and test circuits..
CO7. Be familiarized with the concept of FPAA and implement different mathematical functions on FPAA platform.

List of Lab Assignments:

List of Lab assignments with LTSpice and cadence virtuoso:

1. i) Familiar with VLSI Design Tools like: LTSpice and cadence virtuoso.
   ii) Design the schematic of an Inverter using **cadence virtuoso** and verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

2. Design and simulate the schematic of the common source amplifier. And verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

3. Design and simulate the schematic of the common drain amplifier, and perform the physical verification for the layout of the same. Verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

4. Design and simulate the schematic of a stage differential amplifier and perform the physical verification for the layout of the same. Verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

5. Design and simulate the schematic of the operational amplifier and perform the physical verification. Verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

6. Design and simulate the schematic of the of cascode current mirror and perform the physical verification. Verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

7. Design and simulate the schematic of wilson current mirror and perform the physical verification. Verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

8. Implement i) adders/Subtractors, Multipliers, Differentiators, Integrators, ii) discrete analog filter using FPAA kit

References:

1.Razavi, B., “Design of Analog CMOS Integrated Circuits”, 1st Ed., McGraw Hill.2001
2.Gray, P.R., Hurst, P. J., Lewis, S.H., Meyer, R.G.,“Analysis and Design of Analog Integrated Circuits”, 4th Ed., John Wiley and Sons. 2001

3..Ramon Pallas-Areny, John G.Webster, " Analog Signal Processing", Willey Student Edition.
4.. AN231E04 Datasheet Rev 1.3
5.. A Programmable and Configurable Mixed-Mode FPAA SoC, Jennifer Hasler et al., Georgia Tech., January 7, 2016". doi:10.1109/TVLSI.2015.2504119.
6. David Johns and Ken Martin, "Switched -Capacitor Circuits", Lecture notes :University of Toronto, (johns@eecg.toronto.edu)/ (martin@eecg.toronto.edu).
7. Amitabha Sinha, "Lecture Notes on Switched Capacitor", MAKAUT

MVDL292: VLSI Design Verification and Testing Lab	**Lecture/Week:4**	**Credit:2**

Course Outcomes:
At the end of this course, students will be able to:
CO1: familiar with Front end design and verification techniques and with System Verilog for verification & EDA tools (Cadence, Mentor Graphics) for creating reusable test environments.
CO2: be familiarized with test bench and acquire hands-on skill for design verification of combinatorial and sequential logic circuits.
CO3: develop skill to write software for testing Combinatorial and Sequential logic circuits
CO4: Write HDL (Verilog/VHDL/ System Verilog) code to test i) a memory chip. ii) to test "**stuck-At faults** "and iii) **"bridging faults"** for MOS transistors
CO5: acquire hands-on skill for debugging digital, analog and mix signal VLSI circuits (CPU, FPAA, ADC etc.) using JTAG.
CO6: develop environment for DSP based testing of mixed signal circuit

List of Experiments:

1. Familiarity with System Verilog for Verification & EDA tools (Cadence, Mentor Graphics).
2. Verify the design of combinatorial logic circuits (8-bit Ripple carry Adder/ 8-bit pipelined Multiplier circuit) using Test Bench method by EDA tools.
3. Do experiment 2 for mod 16 binary counter
4&5. Write an HDL code (using Verilog/VHDL/System "C") for verifying a combinatorial/sequential circuit: a) Apply a set of test stimuli to the inputs of the circuit under test (CUT).
b) Check the output response for all input stimuli.
6 & 7. Write a Verilog/VHDL/ System Verilog code to Test i) a memory chip. ii) to test "**stuck-At faults** "and iii) **"bridging faults"** for MOS transistors.
Experimental Set Up: Use a bread board/Vero board and develop a small circuit to interface a) memory chip b) MOS transistors with PC through parallel port/ U.S.B.
8. Experimental Set Up: Interface a Microprocessor/ DSP Processor board with a PC through JTAG port and using boundary scan technique to test the Processor on various input stimuli.
9. Experimental Set Up: Interface an Analog/Mixed Signal circuit board (FPAA) with a PC through JTAG port and using boundary scan technique test the circuit on various input stimuli.
10 &11. Set up an experiment for DSP based Mixed signal Test:
Required Hardware boards and Software tools: 1) PC 2) DSP board 3) ADC and DAC IC Chips 3) Vero board 4) Software tools: Verilog / C /System C

References:

1. N. K. Jha et.al.,"Testing of Digital Systems"
3. M Abramovici and A D Friedman. , " Digital Systems Testing and Testable Design"
3..M. L. Bushnell and V.D. Agrawal, Essentials of Electronic Testing for Digital Memory and

Mixed Signal VLSI Circuits, Springer, 2005.
4. M. Abramovici, M. Breuer, and A. Friedman, *Digital System Testing and Testable Design*, IEEE Press, 1994
5.Chris Spears, " System Verilog for Verification", Springer, 2nd Edition
6.M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory andMixed-Signal VLSI Circuits", Kluwer Academic Publishers
7.IEEE 1800-2009 standard (IEEE Standard for System Verilog— Unified HardwareDesign Specification, and Verification Language).
8. Amitabha Sinha, "Lecture notes on Testing & Verification of VLSI circuits", MAKAUT.

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Semester III

MVDP301A Introduction to AI , Machine Learning and Applications	
Teaching Scheme	**Lecture per week: 3** **Credit: 3**

Course Outcomes:

At the end of the course, students will be able to:

CO1: Learn the basic concept of Artificial Intelligence, Machine Learning , Neural network and their inter-relations different AI techniques

CO2: Learn the concept of Knowledge Representation and knowledge representation issues and the concept of Logic programming.

CO3: Learn the concept of Reasoning under uncertainty for Artificial Intelligence

CO4: Learn the basic concept of Biological Network and modelling of Artificial Neural Network.

CO5: Learn the concept of Machine Learning and different types of Machine Learning Network

CO6: Learn the Architecture of Convolutional Neural Network (CNN) & it's application to Image classification and VLSI implementation of Machine Learning Engine.

Syllabus Contents:

MODULE 1: Introduction to AI, Machine Learning, Deep Learning and Neural Network and their inter relation, Machine Learning vs Neural Network and key differences,

The AI Problems, The Underlying Assumption, AI Techniques, Level of The Model, Criteria For Success, Some General References, One Final Word Problems, State Space Search & Heuristic Search Techniques: Defining The Problems as a State Space Search, Production Systems, Production Characteristics, Production System Characteristics, Issues In The Design Of Search Programs, Additional Problems. Generate-And-Test, Hill Climbing, Best-First search and Breadth-first Search, \ Problem Reduction, Constraint Satisfaction, Means-Ends Analysis.

MODULE 2:

Knowledge Representation Issues: Representations And Mappings, Approaches To Knowledge Representation. Using Predicate Logic: Representation Simple Facts In Logic, Representing Instance And Isa Relationships, Computable Functions And Predicates, Resolution. Representing Knowledge Using Rules: Procedural Versus Declarative Knowledge, Logic Programming, Forward Versus Backward Reasoning.

MODULE 3:

Symbolic Reasoning under uncertainty: Introduction To No monotonic Reasoning, Logics For Non-monotonic Reasoning. Statistical Reasoning: Probability And Bays' Theorem, Certainty Factors And Rule-Base Systems, Bayesian Networks, Dempster Shafer Theory

MODULE 4:

Concept and structure and functions of Biological Neuron, introduction to function of Human Brain, Characteristics of Biological Neural Network, Introduction to Artificial Neural Network (ANN), Non-Linear Characteristics, model of an Artificial Neural Network, Properties of ANN, Layers and structures

of ANN, Forward and Back Propagation NN, Different Activation Functions,

MODULE 5:
Concept of Learning, Machine Learning and key elements, Different types of machine Learning: Supervised learning Unsupervised learning, Semi-supervised learning, Reinforcement learning, Adaptive Learning, Difference between traditional programming and machine Learning. Deep Learning Network, Concept of Convolution and Convolutional Neural Network (CNN), Layers of CNN: Pooling Layer, Max Pooling Layer, Global average Pooling Layer, Normalization Layer, Fully-Connected Layer , Converting Fully Connected Layers to Convolutional Layers, different Activation Layers.

MODULE 6:

Architecture of CNN: Layer Patterns ,Layer Sizing Patterns , Image Classification using CNN: CNN Architecture of Image Classification ,concept of activation Layer RELU ,Details about CNN, Stages of CNN, concepts of Filters, Stride, Padding, Filter hyperparameters, Parameter Sharing
Filter Activations: Feature maps, Soft Max Function, Computational considerations.
Efficient Hardware Realization for Neural Networkof CNN, Reconfigurable VLSI Architecture of CNN, Concept and need of Reconfigurability, VLSI AI Engines to Provide Compute Density for Machine Learning, Case studies (Xilinx AI engine), Concept of" Near Memory Computing" and Analog VLSI for implementing Machine Learning Systems, Neural Network training using Analog Memory, State-of-the-art Analog Deep Machine Learning Systems.

Text Books:

1. Munesh Trivedi, A Classical Approach to Artificial Intelligence, Khanna Publishing House.

2. Elaine Rich and Kevin Knight "Artificial Intelligence", 2nd Edition, Tata McGraw-Hill, 2005.

3.Stuart Russel and Peter Norvig, "Artificial Intelligence: A Modern Approach", 3rd Edition, Prentice Hall, 2009

4. Jeeva Jose, Machine Learning, Khanna Book Publishing House.

References:

1. Amitabha Sinha , " AI. Machine Learning & Applications in Image Classifications", MAKAUT
2. Jianxin Wu ,"Introduction to Convolutional Neural Networks", LAMDA Group National Key Lab for Novel Software Technology Nanjing University, China wujx2001@gmail.com May 1, 2017 (https://cs.nju.edu.cn/wujx/paper/CNN.pdf)
3. https://towardsdatascience.com/an-introduction-to-convolutional-neural-networks-eb0b60b58fd7
4. Himadri Sankar Chatterjee,"A Basic Introduction to Convolutional Neural Network", https://medium.com/@himadrisankarchatterjee/a-basic-introduction-to-convolutional-neural-network-8e39019b27c4
5. Rajiv Chopra, Machine Learning, Khanna Book Publishing House.

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MVDP301B Selected Topics in Engineering Mathematics

Course Outcomes:

At the end of the course, students will be able to:

- Characterize and represent data collected from experiments using statistical methods.
- Model physical process/systems with multiple variables towards parameter estimation andprediction
- Represent systems/architectures using graphs and trees towards optimizing desired objective

Syllabus Contents:

Unit 1: Probability and Statistics:

- Definitions, conditional probability, Bayes Theorem and independence.
- Random Variables: Discrete, continuous and mixed random variables, probability mass, probability density and cumulative distribution functions, mathematical expectation, moments, moment generating function, Chebyshev inequality.

Unit 2: Special Distributions: Discrete uniform, Binomial, Geometric, Poisson, Exponential, Gamma, Normal distributions.

- Pseudo random sequence generation with given distribution, Functions of a Random Variable

Unit 3: Joint Distributions: Joint, marginal and conditional distributions, product moments, correlation, independence of random variables, bi-variate normal distribution.

- Stochastic Processes: Definition and classification of stochastic processes, Poisson process
- Norms, Statistical methods for ranking data

Unit 4: Multivariate Data Analysis

- Linear and non-linear models, Regression, Prediction and Estimation
- Design of Experiments – factorial method
- Response surface method

Unit 5: Graphs and Trees:

- Graphs: Basic terminology, multi graphs and weighted graphs, paths and circuits, shortest path Problems, Euler and Hamiltonian paths and circuits, factors of a graph, planar graph and Kuratowski's graph and theorem, independent sets, graph colouring

Unit 6: Trees: Rooted trees, path length in rooted trees, binary search trees, spanning trees and cut set,theorems on spanning trees, cut sets , circuits, minimal spanning trees, Kruskal's and Prim's algorithms for minimal spanning tree

References:

- Henry Stark, John W. Woods, "Probability and Random Process with Applications to Signal Processing", Pearson Education, 3rd Edition
- C. L. Liu, "Elements of Discrete Mathematics", Tata McGraw-Hill, 2nd Edition
- Douglas C. Montgomery, E.A. Peck and G. G. Vining, "Introduction to Linear Regression Analysis", John Wiley and Sons, 2001.
- Douglas C. Montgomery, "Design and Analysis of Experiments", John Wiley and Sons, 2001.
- B. A. Ogunnaike, "Random Phenomena: Fundamentals of Probability and Statistics for Engineers", CRC Press, 2010.
- S.B. Singh, Discrete Structures, Khanna Book Publishing House.

MVDP301C : Nanomaterials 7 Nanotechnology	**Lecture/Week:3**	**Credit:3**	

Course Outcomes:

- At the end of the course, students will be able to:
  CO1: To understand the basic science behind the design and fabrication of nano scalesystems.
  CO2: To understand and formulate new engineering solutions for current problems and competing technologies for future applications.
  CO3: To be able make inter disciplinary projects applicable to wide areas by clearing andfixing the boundaries in system development.
  CO4: To gather detailed knowledge of the operation of fabrication and characterization devices to achieve precisely designed systems

Syllabus Contents:

Unit 1: Nanomaterials in one and higher dimensions,

Unit 2: Applications of one and higher dimension nano-materials.

Unit 3: Nano-lithography, micro electro-mechanical system (MEMS) and nano-phonics.

Unit 4:carbon nanotubes – synthesis and applications

Unit 5 and 6: Interdisciplinary arena of nanotechnology.

References:

- Nanoscale Materials in Chemistry edited by Kenneth J. Klabunde and Ryan M. Richards,2nd edn, John Wiley and Sons, 2009.
- Nanocrystalline Materials by A I Gusev and A ARempel, Cambridge InternationalScience Publishing, 1st Indian edition by Viva Books Pvt. Ltd. 2008.
- Springer Handbook of Nanotechnology by Bharat Bhushan, Springer, 3rdedn, 2010.
- Carbon Nanotubes: Synthesis, Characterization and Applications by Kamal K. Kar,Research Publishing Services; 1stedn, 2011, ISBN-13: 978-9810863975.

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MVDP301D : Low Power VLSI Design	**Lecture/Week:3**	**Credit:3**

Course Outcomes:
At the end of this course, students will be able to

- CO1: Identify the sources of power dissipation in digital IC systems & understand theimpact of power on system performance and reliability.
- CO2: Characterize and model power consumption & understand the basic analysis methods
- CO3: Learn low power clock distribution
- CO4: Learn Synthesis for low Power estimation and minimization technique and circuits design styles for various arithmetic and logical units.
- CO5: To learn the technique of low power Memory design.
- CO6: To learn the technique of low power microprocessor design and Power Management.

Syllabus Contents:

MODULE 1: Technology & Circuit Design Levels: Sources of power dissipation in digital ICs, degree of freedom, recurring themes in low-power, emerging low power approaches, dynamic dissipation in CMOS, effects of Vdd & Vt on speed, constraints on Vt reduction, transistor sizing & optimal gate oxide thickness, impact of technology scaling, technology innovations.

MODULE2: Low Power Circuit Techniques: Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches.

MODULE 3: Low Power Clock Distribution: Power dissipation in clock distribution, single driver versus distributed buffers, buffers & device sizing under process variations, zero skew Vs. tolerable skew, chip & package co-design of clock network.

MODULE 4: Logic Synthesis for Low Power estimation techniques: Power minimization techniques, low power arithmetic components- circuit design styles, adders, multipliers.

MODULE 5: Low Power Memory Design: Sources & reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM & SRAM, low power DRAM circuits,low power SRAM circuits.

MODULE 6: Low Power Microprocessor Design System: power management support, architectural tradeoffs for power, choosing the supply voltage, low-power clocking, implementation problem for low power, comparison of microprocessors for power & performance.

Text Books:

1.P. Rashinkar, Paterson and L. Singh, “Low Power Design Methodologies”, Kluwer Academic, 2002
2.Kaushik Roy, Sharat Prasad, “Low power CMOS VLSI circuit design”, John Wiley sons Inc.,2000.
3.J.B.Kulo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley, 1999.

References:

4.A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer,1995
5.Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998

Lab: MVDL391: Machine learning Using Python Programming	**Lecture/Week:4**	**Credit:2**

Outcome:

After completion of the lecture as well as laboratory classes , students will able to ,

CO1: learn the core programming basics—including data types, control structures, algorithm development, and program design with functions—via the Python programming language.
CO2: learn the fundamental principles of Object-Oriented Programming, as well as in-depth data and information processing techniques.
CO3: solve problems, explore real-world software development challenges, and create practical and contemporary applications.
CO4: develop algorithm and write program for machine learning using Python.

Syllabus contents:

1.**Lectures on specific topic coverage includes:**

- Algorithms and Information Processing
- Control Structures
- Boolean logic and Numeric Data Types
- Strings, Text Files, Lists, and Dictionaries
- Procedural Abstraction in Function Definitions
- Objects and Classes
- Graphics and Image Processing
- Networks and Client/Server Programming
- Graphic User Interfaces (GUI)
- Events and Event-driven Programming

Lectures on
Module 1: Conceptual introduction: topics in computer science, algorithms; data representation in computers, software and operating system; installing Python; basic syntax, interactive shell, editing, saving, and running a script.
The concept of data types; variables, assignments; immutable variables;
numerical types; arithmetic operators and expressions; comments in the program; understanding error messages; Conditions, boolean logic, logical operators; ranges; Control statements: if-else, loops (for, while); short-circuit (lazy) evaluation. Searching, Sorting, and Complexity Analysis

Module 2: Strings and text files; manipulating files and directories, os and sys modules; text files: reading/writing text and numbers from/to a file; creating and reading a formatted file (csv or tab-separated). String manipulations: subscript operator, indexing, slicing a string; strings and number

system: converting strings to numbers and vice versa.Binary, octal, hexadecimal numbers Lists, tuples, and dictionaries; basic list operators, replacing, inserting, removing an element; searching and sorting lists; dictionary literals, adding and removing keys, accessing and replacing values; traversing dictionaries.

Module 3 : Design with functions: hiding redundancy, complexity; arguments and return values; formal vs actual arguments, named arguments. Program structure and design. Recursive functions. Simple Graphics and Image Processing: "turtle" module; simple 2d drawing - colors, shapes; digital images, image file formats, image processing Simple image manipulations with 'image' module (convert to bw, greyscale, blur, etc).

Module 4: Classes and OOP: classes, objects, attributes and methods; defining classes; design with classes, data modeling; persistent storage of objects.: inheritance, polymorphism, operator overloading (_eq_,_str_, etc); abstract classes; exception handling, try block.
: Graphical user interfaces; event-driven programming paradigm; tkinter module, creating simple GUI; buttons, labels, entry fields, dialogs; widget attributes - sizes, fonts, colors layouts, nested fram

Module 5: Multithreading, Networks, and Client/Server Programming; introduction to HTML, interacting with remote HTML server, running html-based queries, downloading pages; CGI programming, programming a simple CGI form.

Assignment 1: Write Python Codes for different types of activation Functions:

a) Write code to generate Sigmoid activation function: $\mathbf{f(x) = 1/(1+e^{-x})}$
b) Write code to generate Hyperbolic Tangent activation function **f(x)= tanh (x)**
c) Write code to generate ReLU (Rectified Linear unit) Activation function
d) Write code to generate Soft Max Activation function

Assignment 2: Write python program to perform convolution operation between a colour image function of size **(7X7X3**) and a filter(kernel) function **(3X3X3)** .to produce a **Feature Map**..

Assignment 3: Write code to draw plot for loss between the training set and testing set.

Assignment 4: Write Python codes to model a **Fully-Connected Layer** to make class predictions using activation functions **1) Sigmoid and 2) Softmax.**

Assignment 5: Write code to draw plot for loss between the training set and testing set.

Assignment 6: Write python code for simulating a Convolutional Neural Network for image classification.

Assignment N: Write python code for Convolutional Neural Network

Textbook:

1. F Kenneth Lambert , "undamentals of Python: First Programs", Publisher: Course Technology, Cengage Learning, 2012 ISBN-13: 978-1-111-82270-5.
2. J. Jose , "Introduction to Computing and Problem Solving with Python ", Khanna Publications
3. Reema Thareja , "Python Programming" , Pearson

Reference Books:

4. Taming Python by Programming, Jeeva Jose, Khanna PublishingHouse
5. Learn Python The Hard Way, Zed A. Shaw, ADDISON-WESLEY
6. Learning Python, Mark Lutz, O'REILY
7. Programming In Python, Dr. Pooja Sharma, BPB

Python Programming - Using Problem Solving Approach, ReemaThareja, OXFORD UNIVERSITY PRESS

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(Dissertation) Dissertation Phase – I and Phase - II
Teaching Scheme Lab work : 20 and 32 hrs/week
Course Outcomes: At the end of this course, students will be able to 1. Ability to synthesize knowledge and skills previously gained and applied to an in-depth study and execution of new technical problem. 2. Capable to select from different methodologies, methods and forms of analysis to produce a suitable research design, and justify their design. 3. Ability to present the findings of their technical solution in a written report. 4. Presenting the work in International/ National conference or reputed journals.
Syllabus Contents: Syllabus Contents: The dissertation / project topic should be selected / chosen to ensure the satisfaction of the urgent need to establish a direct link between education, national development and productivity and thus reduce the gap between the world of work and the world of study. The dissertation should have the following Relevance to social needs of society Relevance to value addition to existing facilities in the institute Relevance to industry need Problems of national importance Research and development in various domain The student should complete the following: Literature survey Problem Definition Motivation for study and Objectives Preliminary design / feasibility / modular approaches Implementation and Verification Report and presentation The dissertation stage II is based on a report prepared by the students on dissertation allotted to them. It may be based on: Experimental verification / Proof of concept. Design, fabrication, testing of Communication System. The viva-voce examination will be based on the above report and work

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Guidelines for Dissertation Phase – I and II at M. Tech. (Electronics):
1. As per the AICTE directives, the dissertation is a year long activity, to be carried out and evaluated in two phases i.e., Phase – I: July to December and Phase – II: January to June.
2. The dissertation may be carried out preferably in-house i.e., departments laboratories and centers OR in industry allotted through departments T & P coordinator.
3. After multiple interactions with guide and based on comprehensive literature survey, the student shall identify the domain and define dissertation objectives. The referred literature should preferably include IEEE/IET/IETE/Springer/Science Direct/ACM journals in the areas of Computing and Processing (Hardware and Software), Circuits-Devices and Systems, Communication-Networking and Security, Robotics and Control Systems, Signal Processing and Analysis and any other related domain. In case of Industry sponsored projects, the relevant application notes, while papers, product catalogues should be referred

and reported.
4. Student is expected to detail out specifications, methodology, resources required, critical issues involved in design and implementation and phase wise work distribution, and submit the proposal within a month from the date of registration.
5. Phase – I deliverables: A document report comprising of summary of literature survey, detailed objectives, project specifications, paper and/or computer aided design, proof of concept/functionality, part results, A record of continuous progress.
6. Phase – I evaluation: A committee comprising of guides of respective specialization shall assess the progress/performance of the student based on report, presentation and Q & A. In case of unsatisfactory performance, committee may recommend repeating the Phase-I work.
7. During phase – II, student is expected to exert on design, development and testing of the proposed work as per the schedule. Accomplished results/contributions/innovations should be published in terms of research papers in reputed journals and reviewed focused conferences OR IP/Patents.
8. Phase – II deliverables: A dissertation report as per the specified format, developed system in the form of hardware and/or software, A record of continuous progress.
9. Phase – II evaluation: Guide along with appointed external examiner shall assess the progress/performance of the student based on report, presentation and Q & A. In case of unsatisfactory performance, committee may recommend for extension or repeating the work

OPEN ELECTIVES

Business Analytics

Teaching scheme

Lecture: - 3 h/week

Total Number of Lectures: 48

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Corse Objective:

1. Understand the role of business analytics within an organization.
2. Analyze data using statistical and data mining techniques and understand relationships between the underlying business processes of an organization.
3. To gain an understanding of how managers use business analytics to formulate and solve business problems and to support managerial decision making.
4. To become familiar with processes needed to develop, report, and analyze business data.
5. Use decision-making tools/Operations research techniques.
6. Mange business process using analytical and management tools.
7. Analyze and solve problems from different industries such as manufacturing, service, retail, software, banking and finance, sports, pharmaceutical, aerospace etc.

LECTURE WITH BREAKUP	NO. OF LECTURES
Unit1: Business analytics: Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of Business Analytics Process and organisation, competitive advantages of Business Analytics. Statistical Tools: Statistical Notation, Descriptive Statistical methods, Review of probability distribution and data modelling, sampling and estimation methods overview.	9
Unit 2: Trendiness and Regression Analysis: Modelling Relationships and Trends in Data, simple Linear Regression. Important Resources, Business Analytics Personnel, Data and models for Business analytics, problem solving, Visualizing and Exploring Data, Business Analytics Technology.	8
Unit 3: Organization Structures of Business analytics, Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, Measuring contribution of Business analytics, Managing Changes. Descriptive Analytics, predictive analytics, predicative Modelling, Predictive analytics analysis, Data Mining, Data Mining Methodologies, Prescriptive analytics and its step in the business analytics Process, Prescriptive Modelling, nonlinear Optimization.	9
Unit 4: Forecasting Techniques: Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonality, Regression Forecasting with Casual Variables, Selecting Appropriate Forecasting Models. Monte Carlo Simulation and Risk Analysis: Monte Carle Simulation	10

Using Analytic Solver Platform, New-Product Development Model, Newsvendor Model, Overbooking Model, Cash Budget Model.	
Unit 5: Decision Analysis: Formulating Decision Problems, Decision Strategies with the without Outcome Probabilities, Decision Trees, the Value of Information, Utility and Decision Making.	8
Unit 6: Recent Trends in: Embedded and collaborative business intelligence, Visual data recovery, Data Storytelling and Data journalism.	4

Course Outcomes:

1. Students will demonstrate knowledge of data analytics.
2. Students will demonstrate the ability of think critically in making decisions based on data and deep analytics.
3. Students will demonstrate the ability to use technical skills in predicative and prescriptive modelling to support business decision-making.
4. Students will demonstrate the ability to translate data into clear, actionable insights.

Reference:

1. Business analytics Principles, Concepts, and Applications by Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, Pearson FT Press.
2. Business Analytics by James Evans, persons Education.

OPEN ELECTIVES

Industrial Safety

Teaching scheme

Lecture: - 3 h/week

Unit-I: Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.

Unit-II: Fundamentals of maintenance engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

Unit-III: Wear and Corrosion and their prevention: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

Unit-IV: Fault tracing: Fault tracing-concept and importance, decision treeconcept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic,automotive, thermal and electrical equipment's like, I. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.

Unit-V: Periodic and preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

Reference:

1. Maintenance Engineering Handbook, Higgins & Morrow, Da Information Services.
2. Maintenance Engineering, H. P. Garg, S. Chand and Company.
3. Pump-hydraulic Compressors, Audels, Mcgrew Hill Publication.
4. Foundation Engineering Handbook, Winterkorn, Hans, Chapman & Hall London.

OPEN ELECTIVES
Operations Research
Teaching Scheme
Lectures: 3 hrs/week

Course Outcomes: At the end of the course, the student should be able to

1. Students should able to apply the dynamic programming to solve problems of discreet and continuous variables.
2. Students should able to apply the concept of non-linear programming
3. Students should able to carry out sensitivity analysis
4. Student should able to model the real-world problem and simulate it.

Syllabus Contents:

Unit 1:
Optimization Techniques, Model Formulation, models, General L.R Formulation, Simplex Techniques, Sensitivity Analysis, Inventory Control Models

Unit 2
Formulation of a LPP - Graphical solution revised simplex method - duality theory - dual simplex method - sensitivity analysis - parametric programming

Unit 3:
Nonlinear programming problem - Kuhn-Tucker conditions min cost flow problem - max flow problem - CPM/PERT

Unit 4
Scheduling and sequencing - single server and multiple server models - deterministic inventory models - Probabilistic inventory control models - Geometric Programming.

Unit 5
Competitive Models,Single and Multi-channel Problems, Sequencing Models, Dynamic Programming, Flow in Networks, Elementary Graph Theory, Game Theory Simulation

References:

1. H.A. Taha, Operations Research, An Introduction, PHI, 2008
2. H.M. Wagner, Principles of Operations Research, PHI, Delhi, 1982.
3. J.C. Pant, Introduction to Optimisation: Operations Research, Jain Brothers, Delhi, 2008
4. Hitler Libermann Operations Research: McGraw Hill Pub. 2009
5. Pannerselvam, Operations Research: Prentice Hall of India 2010
6. Harvey M Wagner, Principles of Operations Research: Prentice Hall of India 2010

Open Elective

Cost Management of Engineering Projects
Teaching scheme
Lecture: - 3 h/week

Introduction and Overview of the Strategic Cost Management Process

Cost concepts in decision-making; Relevant cost, Differential cost, Incremental cost and Opportunity cost. Objectives of a Costing System; Inventory valuation; Creation of a Database for operational control; Provision of data for Decision-Making.
Project: meaning, Different types, why to manage, cost overruns centres, various stages of project
execution: conception to commissioning. Project execution as conglomeration of technical and non-technical activities. Detailed Engineering activities. Pre project execution main clearances and documents Project team: Role of each member. Importance Project site: Data required with significance. Project contracts. Types and contents. Project execution Project cost control. Bar charts and Network diagram. Project commissioning: mechanical and process

Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis. Various decision-making problems. Standard Costing and Variance Analysis. Pricing strategies: Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector. Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning, Total Quality Management and Theory of constraints. Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis. Budgetary Control; Flexible Budgets; Performance budgets; Zero-based budgets. Measurement of Divisional profitability pricing decisions including transfer pricing.

Quantitative techniques for cost management, Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Simulation, Learning Curve Theory.

References:

2. Cost Accounting A Managerial Emphasis, Prentice Hall of India, New Delhi
3. Charles T. Horngren and George Foster, Advanced Management Accounting
4. Robert S Kaplan Anthony A. Alkinson, Management & Cost Accounting
5. Ashish K. Bhattacharya, Principles & Practices of Cost Accounting A. H. Wheeler publisher
6. N.D. Vohra, Quantitative Techniques in Management, Tata McGraw Hill Book Co. Ltd.

Open Elective
Composite Materials
Teaching scheme
Lecture: - 3 h/week

UNIT–I: INTRODUCTION: Definition – Classification and characteristics of Composite materials Advantages and application of composites. Functional requirements of reinforcement and matrix. Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance.
UNIT – II: REINFORCEMENTS: Preparation-layup, curing, properties and applications of glass fibers, carbon fibers, Kevlar fibers and Boron fibers. Properties and applications of whiskers, particle reinforcements. Mechanical Behavior of composites: Rule of mixtures, Inverse rule of mixtures. Isostrain and Isostress conditions.
UNIT – III: Manufacturing of Metal Matrix Composites: Casting – Solid State diffusion technique, Cladding – Hot isostatic pressing. Properties and applications. Manufacturing of Ceramic Matrix Composites: Liquid Metal Infiltration – Liquid phase sintering. Manufacturing of Carbon – Carbon composites: Knitting, Braiding, Weaving. Properties and applications.
UNIT–IV: Manufacturing of Polymer Matrix Composites: Preparation of Moulding compounds and prepregs – hand layup method – Autoclave method – Filament winding method – Compression moulding – Reaction injection moulding. Properties and applications.
UNIT – V: Strength: Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygrothermal failure. Laminate first play failure-insight

strength; Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots; stress concentrations.

TEXT BOOKS:

1. Material Science and Technology – Vol 13 – Composites by R.W.Cahn – VCH, West Germany.
2. Materials Science and Engineering, An introduction. WD Callister, Jr., Adapted by R. Balasubramaniam, John Wiley & Sons, NY, Indian edition, 2007.

References:

1. Hand Book of Composite Materials-ed-Lubin.
2. Composite Materials – K.K.Chawla.
3. Composite Materials Science and Applications – Deborah D.L. Chung.
4. Composite Materials Design and Applications – Danial Gay, Suong V. Hoa, and Stephen W. Tasi.

Open Elective
Waste to Energy

Teaching scheme
Lecture: - 3 h/week

Unit-I: Introduction to Energy from Waste: Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors
Unit-II: Biomass Pyrolysis: Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.
Unit-III: Biomass Gasification: Gasifiers – Fixed bed system – Downdraft and updraft gasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation.
Unit-IV: Biomass Combustion: Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.
Unit-V: Biogas: Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme in India.

References:

1. Energy Technology, O.P. Gupta, Khanna Publishing House.
2. Non-Conventional Energy, Desai, Ashok V., Wiley Eastern Ltd., 1990.

3. Biogas Technology - A Practical Hand Book - Khandelwal, K. C. and Mahdi, S. S., Vol. I & II, Tata McGraw Hill Publishing Co. Ltd., 1983.
4. Food, Feed and Fuel from Biomass, Challal, D. S., IBH Publishing Co. Pvt. Ltd., 1991.
5. Biomass Conversion and Technology, C. Y. WereKo-Brobby and E. B. Hagan, John Wiley & Sons, 1996.

AUDIT 1 and 2: ENGLISH FOR RESEARCH PAPER WRITING

Course objectives:
Students will be able to:
1. Understand that how to improve your writing skills and level of readability
2. Learn about what to write in each section
3. Understand the skills needed when writing a Title Ensure the good quality of paper at very first-time submission.

Syllabus

1. Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness (4)
2. Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticising, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction (4)
3. Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check. (4)
4. key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature, (4)
5. skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions 4
6. useful phrases, how to ensure paper is as good as it could possibly be the first- time submission (4).

Suggested Studies:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book .
4. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011,

AUDIT 1 and 2: DISASTER MANAGEMENT

Course Objectives: -

Students will be able to:

1. learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
2. critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
3. develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
4. critically understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countries they work in.

Syllabus

1 Introduction Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude. (4)

2 Repercussions of Disasters and Hazards: Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts. (4)

3 Disaster Prone Areas In India Study Of Seismic Zones; Areas Prone To Floods And Droughts, Landslides And Avalanches; Areas Prone To Cyclonic And Coastal Hazards With Special Reference To Tsunami; Post-Disaster Diseases And Epidemics (4).

4 Disaster Preparedness and Management Preparedness: Monitoring Of Phenomena Triggering A Disaster Or Hazard; Evaluation Of Risk: Application Of Remote Sensing, Data From Meteorological And Other Agencies, Media Reports: Governmental And Community Preparedness. (4)

5 Risk Assessment Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques Of Risk Assessment, Global Co-Operation In Risk Assessment And Warning, People's Participation In Risk Assessment. Strategies for Survival. (4)

6 Disaster Mitigation Meaning, Concept and Strategies Of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation In India.

SUGGESTED READINGS:

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'New Royal book Company.
2. S.C. Sharma, Disaster management, Khanna Book Publishing House.
3. Sahni, Pardeep Et.Al. (Eds.)," Disaster Mitigation Experiences And Reflections", Prentice Hall Of India, New Delhi.
4. Goel S. L. , Disaster Administration And Management Text And Case Studies" ,Deep &Deep Publication Pvt. Ltd., New Delhi

AUDIT 1 and 2: SANSKRIT FOR TECHNICAL KNOWLEDGE

Course Objectives

1. To get a working knowledge in illustrious Sanskrit, the scientific language in the world
2. Learning of Sanskrit to improve brain functioning
3. Learning of Sanskrit to develop the logic in mathematics, science & other subjects enhancing the memory power
4. The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from ancient literature

Syllabus Content

1 • Alphabets in Sanskrit
  • Past/Present/Future Tense,
  • Simple Sentences (8)
2 • Order
  • Introduction of roots
  • Technical information about Sanskrit Literature (8)
3 • Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics

Suggested reading

1. "Abhyaspustakam" – Dr.Vishwas, Samskrita-Bharti Publication, New Delhi
2. "Teach Yourself Sanskrit" Prathama Deeksha-Vempati Kutumbshastri, Rashtriya Sanskrit Sansthanam, New Delhi Publication
3. "India's Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., New Delhi.

Course Output

Students will be able to

1. Understanding basic Sanskrit language

2. Ancient Sanskrit literature about science & technology can be understood
3. Being a logical language will help to develop logic in students

AUDIT 1 and 2: VALUE EDUCATION

Course Objectives
Students will be able to
1.Understand value of education and self- development
2. Imbibe good values in students
3. Let they should know about the importance of character

Syllabus Contents:

1. Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism. • Moral and non- moral valuation. Standards and principles. • Value judgements [4].

2 Importance of cultivation of values. • Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. • Honesty, Humanity. Power of faith, National Unity. • Patriotism. Love for nature, Discipline [6]

3 Personality and Behaviour Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline. • Punctuality, Love and Kindness. • Avoid fault Thinking. • Free from anger, Dignity of labour. • Universal brotherhood and religious tolerance. • True friendship. • Happiness Vs suffering, love for truth. • Aware of self-destructive habits. • Association and Cooperation. • Doing best for saving nature [6]

4 Character and Competence –Holy books vs Blind faith. • Self-management and good health. • Science of reincarnation. • Equality, Nonviolence, Humility, Role of Women. • All religions and same message. • Mind your Mind, Self-control. • Honesty, Studying effectively

Suggested reading
1 Chakroborty, S.K. “Values and Ethics for organizations Theory and practice”, Oxford University Press, New Delhi
2 Premvir Kapoor, Professional Ethics and Human Values, Khanna Book Publishing House

Course outcomes
Students will be able to
1.Knowledge of self-development
2.Learn the importance of Human values
3.Developing the overall personality.

Maulana Abul Kalam Azad University of Technology, West Bengal
(Formerly West Bengal University of Technology)
Syllabus of M. Tech. (Electronics & Communication Engineering): Specialization: VLSI Design
(Effective from academic session 2021-22)

AUDIT 1 and 2: CONSTITUTION OF INDIA

Course Objectives:

Students will be able to:
1. Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
2. To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
3. To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.

Syllabus Contents:

1. History of Making of the Indian Constitution: History Drafting Committee, (Composition & Working) (4)
3 Philosophy of the Indian Constitution: Preamble, Salient Features (4)
3. Contours of Constitutional Rights & Duties:
- Fundamental Rights
- Right to Equality
- Right to Freedom
- Right against Exploitation
- Right to Freedom of Religion
- Cultural and Educational Rights
- Right to Constitutional Remedies
- Directive Principles of State Policy
- Fundamental Duties.

(4)

4. Organs of Governance:
- Parliament
- Composition
- Qualifications and Disqualifications
- Powers and Functions
- Executive
- President
- Governor
- Council of Ministers

- Judiciary, Appointment and Transfer of Judges, Qualifications
- Powers and Functions

(4)

5. Local Administration:
- District's Administration head: Role and Importance,
- Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation.
- Pachayati raj: Introduction, PRI: Zila Pachayat.
- Elected officials and their roles, CEO Zila Pachayat: Position and role.
- Block level: Organizational Hierarchy (Different departments),
- Village level: Role of Elected and Appointed officials,
- Importance of grass root democracy

(4)

6. Election Commission:
- Election Commission: Role and Functioning.
- Chief Election Commissioner and Election Commissioners.
- State Election Commission: Role and Functioning.
- Institute and Bodies for the welfare of SC/ST/OBC and women.

(4)

Suggested reading

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

Course Outcomes:

Students will be able to:

1. Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
2. Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
3. Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
4. Discuss the passage of the Hindu Code Bill of 1956.

AUDIT 1 and 2: PEDAGOGY STUDIES

Course Objectives:

Students will be able to:

4. Review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers.
5. Identify critical evidence gaps to guide the development.

Syllabus Contents:

1. Introduction and Methodology:
  Aims and rationale, Policy background, Conceptual framework and terminology
  Theories of learning, Curriculum, Teacher education.
  Conceptual framework, Research questions.
  Overview of methodology and searching.
(4)

2. Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries.
  Curriculum, Teacher education.
(4)

3. Evidence on the effectiveness of pedagogical practices
  Methodology for the in depth stage: quality assessment of included studies.
  How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?
  Theory of change.
  Strength and nature of the body of evidence for effective pedagogical practices.
  Pedagogic theory and pedagogical approaches.
  Teachers' attitudes and beliefs and Pedagogic strategies.
(4)

4. Professional development: alignment with classroom practices and follow-up support
  Peer support
  Support from the head teacher and the community.
  Curriculum and assessment
  Barriers to learning: limited resources and large class sizes (4)

5. Research gaps and future directions
  Research design
  Contexts
  Pedagogy
  Teacher education
  Curriculum and assessment
  Dissemination and research impact.
(2)

Suggested reading
1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, 'learning to read' campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

Course Outcomes:

Students will be able to understand:
1. What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries?
2. What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
3. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

AUDIT 1 and 2: STRESS MANAGEMENT BY YOGA

Course Objectives
1. To achieve overall health of body and mind
2. To overcome stress

Syllabus
1 Definitions of Eight parts of yog. (Ashtanga)
2 Yam and Niyam.
Do`s and Don't's in life.
i) Ahinsa, satya, astheya, bramhacharya and aparigraha
ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan
3 Asan and Pranayam
i) Various yog poses and their benefits for mind & body
ii)Regularization of breathing techniques and its effects-Types of pranayam

Suggested reading

1. 'Yogic Asanas for Group Tarining-Part-I" : Janardan Swami Yogabhyasi Mandal, Nagpur
2. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata

Course Outcomes:

Students will be able to:

1. Develop healthy mind in a healthy body thus improving social health also
2. Improve efficiency

AUDIT 1 and 2: PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS

Course Objectives

1. To learn to achieve the highest goal happily
2. To become a person with stable mind, pleasing personality and determination
3. To awaken wisdom in students

Syllabus

1 Neetisatakam-Holistic development of personality
- Verses- 19,20,21,22 (wisdom)
- Verses- 29,31,32 (pride & heroism)
- Verses- 26,28,63,65 (virtue)
- Verses- 52,53,59 (dont's)
- Verses- 71,73,75,78 (do's)

(8)

2 Approach to day to day work and duties.
- Shrimad Bhagwad Geeta : Chapter 2-Verses 41, 47,48,
- Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23, 35,
- Chapter 18-Verses 45, 46, 48.

(8)

3 Statements of basic knowledge.
- Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68
- Chapter 12 -Verses 13, 14, 15, 16,17, 18
- Personality of Role model. Shrimad Bhagwad Geeta: Chapter2-Verses 17, Chapter 3-Verses 36,37,42,
- Chapter 4-Verses 18, 38,39
- Chapter18 – Verses 37,38,63

(8)

Suggested reading

1. "Srimad Bhagavad Gita" by Swami Swarupananda Advaita Ashram (Publication Department), Kolkata

2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi.

Course Outcomes

Students will be able to

1. Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life
2. The person who has studied Geeta will lead the nation and mankind to peace and prosperity
3. Study of Neetishatakam will help in developing versatile personality of students.