MAULANA ABUL KALAM AZAD
UNIVERSITY OF TECHNOLOGY,
WEST BENGAL

THE DEPARTMENT OF
MICROELECTRONICS AND VLSI TECHNOLOGY

SYLLABUS

FOR POST GRADUATE DEGREE COURSE (M.Tech) IN

Embedded Systems &VLSI Design

[November 2021]

M.Tech in Embedded Systems &VLSI Design

VISION OF THE UNIVERSITY

To achieve the status of a globally ranked premier University in the field of Science, Technology, Pharmacy, Architecture, Management and interdisciplinary areas for the creation of high-calibre professionals with environmental consciousness, social, moral and ethical values along with the competency to face the new challenges of rapid technological advancements.

MISSION OF THE UNIVERSITY

To impart quality and value based teaching & learning of international standard for solving the real life problems

- To create and disseminate knowledge both nationally & internationally towards the transformations of the civilization into a knowledge based society
- To institutionalize the extension and field outreach activities with a view to transform the university system into an active instrument for social change
- To develop liaison and collaboration with the globally recognised academic institutions in order to inject new and fresh thinking in teaching, learning and research
- To generate intellectually capable and imaginatively gifted professionals and successful entrepreneurs having environmental consciousness and ethics who can work as individual or in group in multi-cultural global environments for continuing significantly towards the betterment of quality of human life.

Vision of Department of Microelectronics and VLSI Technology

The Department of Microelectronics and VLSI Technology envisions to be a leader in pursuit of knowledge and wisdom for the holistic development of the rapid technological advancements of society in multi-disciplinary areas through excellence in teaching, training, and research and aspires to meet the global and socio economic challenges of the state as well as country.

Mission statements of the Department of Microelectronics and VLSI Technology (MS)

MS-1: The Department of Microelectronics and VLSI Technology motivates to produce globally competent Engineers prepared to face challenges of the society.

MS-2: To enable the students to formulate, design and solve problems in applied science and engineering.

MS-3: To provide excellent teaching and research environment using state of the art facilities.

MS-4: To provide adequate practical training to meet the requirement of the Microelectronics & VLSI industry.

MS-5: To train the students to take up leadership roles in their career or to pursue higher education and research.

Program Educational Objectives (PEOs)

PEO-1: To train students on state-of-the-art Digital and Analog Integrated Circuit(IC) design
PEO-2: To train students on Testing & verification of Digital, Analog and mixed signal ICs.
PEO-3: To learn hardware software co-design for various embedded application development.
PEO-4: To offer training on full cycle development of Integrated circuits, Device design using Electronic Design Automation (EDA) tool.
PEO-5: To train students in analytical reasoning, experimental skills and attitude to collaborate between inter-disciplinary research groups.

Mapping Program Educational Objectives (PEOs) with Mission Statements (MS)

	MS-1	MS-2	MS-3	MS-4	MS-5
PEO-1	3	3	3	3	1
PEO-2	3	3	3	3	1
PEO-3	2	3	3	3	2
PEO-4	2	2	3	3	1
PEO-5	2	3	2	2	2

Note: '3' in the box for 'high-level'mapping, 2 for 'Medium-level'mapping, 1 for 'Low-level' mapping.

Program Outcomes (POs)

After completion of this M.Tech program, the students will be able to

PO-1. Engineering Knowledge: Apply the knowledge of mathematics, science, Engineering fundamentals, and an Engineering specialization to the solution of complex Engineering problems.

PO-2. Problem Analysis : Identify, formulate, review research literature, and analyze complex Engineering problems reaching substantiated conclusions using first principles of mathematics natural sciences, and Engineering sciences.

PO-3. Design/Development of Solutions : Design solutions for complex Engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and Environmental considerations.

PO-4. Conduct Investigations of Complex Problems : Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO-5. Modern Tool Usage : Create, select, and apply appropriate techniques, resources, and modern Engineering and IT tools including prediction and modeling to complex Engineering activities with an understanding of the limitations.

PO-6. The Engineer and Society : Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO-7. Environment and Sustainability: Understand the impact of the professional Engineering solutions in societal and Environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO-8. Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the Engineering practice.

PO-9. Individual and Team Work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO-10. Communication: Communicate effectively on complex Engineering activities with the Engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive

clear instructions.

PO-11. Project Management and Finance: Demonstrate knowledge and understanding of the Engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary Environments.

PO-12. Life - Long Learning : Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes (PSOs)

PSO-1 Design and develop efficient VLSI architectures to implement digital ,analog and mixed signal circuits & systems , Advanced Microprocessors/ Microcontrollers, Digital Signal Processors etc.
PSO-2: Usage of EDA tools for System Design using Programmable digital & analog Hardware (FPGA/FPAA) .
PSO-3: Design & Verification, Simulation, Fabrication and Testing of Digital, Analog and Mixed Signal ICs.
PSO-4: Design of low power ICs, low power Memory devices and MEMS using EDA tools .
PSO-5: **To** learn hardware software co-design for various embedded application development.

Mapping of Program Outcomes (POs) and Program Specific Outcomes (PSOs) with Program Educational Objectives (PEOs)

	PEO-1	PEO-2	PEO-3	PEO-4	PEO-5
PO-1	3	3	3	2	3
PO-2	1	2	2	2	2
PO-3	2	2	2	1	3
PO-4	2	2	2	1	3
PO-5	1	2	2	2	2
PO-6	2	2	2	2	2
PO-7	1	1	2	1	2
PO-8	1	1	2	1	2
PO-9	2	2	3	3	3
PO-10	2	2	3	3	3
PO-11	2	2	3	3	3
PO-12	1	1	2	1	2
PSO-1	3	1	3	3	3
PSO-2	3	1	3	3	3
PSO-3	1	3	3	3	3
PSO-4	3	3	3	3	1
PSO-5	2	2	3	3	2

Note: '3' in the box for 'high-level'mapping, 2 for 'Medium-level'mapping, 1 for 'Low-level' mapping.

Semester-wise Course Schedule:

Semester I

Sr. No.	Course Type/ Code	Course Name	Teaching			Credits
			L	T	p	
1	PGVES - 101	Digital VLSI Design	3	0	0	3
2	PGVES - 102	Microcontrollers and Programmable Digital Signal Processors	3	0	0	3
3	PGVES-103: PE I	Elective I A) Digital Signal and Image Processing B) Programming Languages for Embedded Systems C) VLSI signal processing	3	0	0	3
4	PGVES-104: PE II	Elective II A) Parallel Architecture & Processing B) System Design with Embedded Linux C) CAD of Digital System	3	0	0	3
5	PGVES-105	Research Methodology and IPR	2	0	0	2
6.	PGVES-106 PA I	Audit course	2	0	0	0
7.	PGVES-191	Digital VLSI Design Lab	0	0	4	2
8.	PGVES-192	Micro-controller and Programmable Digital Signal Processor Lab.	0	0	4	2
		Total	**14**	**0**	**8**	**18**

Semester II

Sr. No.	Course Code	Course Name	Teaching Scheme			Credits
			L	T	p	
1	PGVES - 201	Analog VLSI Design	3	0	0	3
2	PGVES - 202	VLSI Design Verification and Testing	3	0	0	3
3	PGVES-203: PE III	Elective III (A) Memory Technologies (B) SOC Design (C) Low power VLSI Design	3	0	0	3
4	PGVES-204: PE IV	Elective IV (A) Communication Buses and Interfaces (B) Introduction to AI , Machine Learning and Applications (C) Physical Design Automation	3	0	0	3
5	PGVES - 291	Analog VLSI Design Lab	0	0	4	2
6	PGVES - 292	VLSI Design Verification and Testing Lab	0	0	4	2
7	PGVES - 281	Mini Project	0	0	4	2
8	PGVES-205	Audit course 2	2	0	0	0
		Total	**14**	**0**	**12**	**18**

Semester-III

Sr. No.	Course Code	Course Name	Teaching Scheme			Credits
1.	PGVES-301: PE V	Elective -V A) Communication Network B) Selected Topics in Mathematics C) Nano Materials and Nanotechnology	3	0	0	3
2.	PGVES - 302: OE VI	A.Business Analytics B. Industrial Safety C. Operations Research D. Cost Management of Engineering Projects E. Composite Materials F. Waste to Energy	3	0	0	3
3	PGVES - 381	M.Tech. Project Phase-I (Dissertation Phase-I)	0	0	20	10
		Total	**6**	**0**	**20**	**16**

Semester-IV

Sr. No.	Course Code	Course Name	Teaching Scheme			Credits
			L	T	p	
I.	PGVES - 481	M.Tech. Project Phase-II (Dissertation Phase-II)	--	--	32	16
		Total	**–**	**–**	**–**	**16**

M.Tech in Embedded Systems &VLSI Design

Semester I

PGVES101:Digital VLSI Design	Lecture/Week:4 (3L,1T) ,Total lectures: 36 Hours	Credit:3

Course Outcomes:

After completion of this course, students will be able to

CO1: Learn the basics of Integrated Circuit (IC),; different Domains of VLSI design, design automation tools and the state-of-the-art VLSI circuits.

CO 2: Learn CMOS logic behaviour, advantages and drawbacks using static, dynamic, Domino logic and Bi-CMOS logic

CO3.Learn the basics of CMOS fabrication and Layout.

CO4: Learn EDA tools and their advantages, concept of test bench, simulation, design verification, synthesis and hardware description language (Verilog/VHDL/System 'C')

CO5: learn the concept of Programmable Hardware and their requirements, FPGA --architecture, configuration and design flow, concept of System on Chip (SOC).

CO6: Learn logical effort, path effort, path effort delay, path parasitic delay, designing fast circuits and multistage logic networks and the concept of delay **vs** fan out,

CO7: Learn the design of a 32-bit RISC CPU, Static RAM and Simulation, Synthesis & validation of the architectures on FPGA and analysis their performances.

MODULE1: Introduction to VLSI Design

Basics of Integrated Circuit (IC), SSI, MSI, LSI, VLSI, ULSI, Integration levels. History of IC development, Moore's Law, Different types of IC chips; Digital, Analog & Mixed signal ICs; Different Domains of VLSI design; EDA- the VLSI design CAD tools, VLSI design state-of-the-art, some emerging applications of VLSI, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay VLSI design of complex processor, VLSI Design Flow, Synthesis, layout generation, Verification and simulation, VLSI chip manufacturing process flow, Radiation-hardened VLSI technology.

MODULE2: CMOS logic Basics

.Basics of MOS transistors and MOS as switches, Complementary CMOS logic , CMOS logic behaviour , advantages and drawbacks of CMOS logic, Pull up and pull down network, conduction complement, complex logic function using CMOS, pass transistors, transmission gates, tri-state buffers, Flip- flops(D- F/F, JK F/F etc.), transistor count, Delay , drawbacks of CMOS, Dynamic logic, Domino logic , Bi-CMOS to overcome the drawbacks of CMOS, standard cell design, full custom design. example of standard cell., combinatorial and Sequential Logic circuits –asynchronous and synchronous sequential circuits , Moore machine, Mealy machine , examples, Finite state machine design ,

MODULE3:Basics of CMOS Layout :

Introduction to VLSI fabrication and fabrication steps, Concept of MASK, Lithography, etching,

polysilicon patterning, ion implementation , metallization etc., fabrication error, concept of layout , feature size, Lamda (λ) rule, concept of process technology , stick diagram, general design rules for layout, width spacing rule, poly diffusion interaction, contacts, VIA and contact spacing, examples of CMOS layout of an inverter, NAND /NOR gates, simplified design rule, full custom and standard cell layout, placement , routing .floor planning ,

MODULE4: Hardware description language & EDA tools

EDA tools and their advantages, concept of test bench, simulation, , design verification , synthesis, hardware description language (HDL) -VHDL/VERILOG/SYSTEM C etc.

MODULE 5: Programmable Hardware and FPGA (6)

Concept of Programmable Hardware (PLA, PLD, CPLD, FPGA) and their requirements, FPGA -- Architecture, configuration and design flow , system design using FPGA , concept of System on Chip(SOC). FPGA as reconfigurable computing and programmable System on Chip(pSOC).

MODULE 6: Logical Effort

Logical effort -Path Logical Effort, Path Electrical Effort , Path Effort , branching effort, , delay in a logic gate, path effort delay, path parasitic delay , designing fast circuits and gate sizes, multistage logic networks, choosing the best number of stages, delay **vs** fan out,

MODULE 7: Example of VLSI chip Design (Design of a 32-bit RISC CPU and 1K8 bit RAM

Designing a RISC CPU with fixed instruction length (32 bit) CPU, few instructions, Static RAM design with 1024 locations with each word size of 8 bits., Simulation, Synthesis & validation of the architecture on FPGA and analysis of the performance of the CPU with a small program written in machine language.

Text Books:

1. Carver Mead, Lynn Conway, Introduction to VLSI Systems", B.S. Publication
2. John P Uyemura ," Chip Design for Submicron VLSI", Thompson Publication.
3. Etienne Scard., Sonia Delmas Bendhia ," Advanced CMOS cell Design :",McGraw Hill Professional .
4. K.V.K.K.Prasad ,Kattula Shyamala, "VLSI Design Black Book", dreamtech Publication
5. Baker,Li,Boyce,"CMOSCircuitDesign,Layout,andSimulation",Wiley,2ndEdition.

References:

1. JP Rabaey, AP Chandrakasan, B Nikolic, "Digital Integrated circuits: A design perspective", Prentice Hall electronics and VLSI series, 2nd Edition.
2. Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation",Wiley,2nd Edition.
3. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits Analysis and Design, McGraw-Hill, 1998.
4. Amitabha Sinha," Lecture Notes on VLSI Design", MAKAUT

PGVES-102: Microcontrollers and Programmable Digital Signal Processors [Sem – I] 3(L)
(36 Lectures) CREDIT-3

Teaching Scheme
Lectures: 3 hrs/week

Course Outcomes: After the completion of this course, students will learn:

CO1. the Concept of Processor Architecture, Data path Design and Control Unit (hardwired control unit, microprogrammed and nano programmed Control unit).
CO2: the Architecture and Programming model of ARM Cortex-M3 Processor/LPC 17xx Microcontroller, the concept of Interrupt with emphasize to interrupt vector, nested interrupt, interrupt chaining, interrupt latency, interrupt controller and efficient handling of interrupts.
CO3: the concept of RISC & CISC Processors, Harvard Architecture and VLIW Architecture.
CO4: to identify and characterize architectural and programming requirements of DSP Processors and to learn the architectural details of Texas Instrument TMS320C67xx series DSP Processors.
CO5: to acquire skills on handling DSP software development platform for application development wi study on code composer studio.

Syllabus Contents:

MODULE 1:

1**. Processor Architecture:**

i) Concept of a Computer Systems, Basic building blocks, Store and forward concept, Von-Neumann Architecture, Introduction to Processor and Processor Organization.

ii) Processor Architecture: Instruction Set Architecture: Instructions & Addressing, Procedures and Data, Instruction Set Variations. (2L)

2. Datapath Design:

i) The Arithmetic/ Logic Unit: Number Representation, Adders and Simple ALUs, Multipliers and Dividers, Floating-Point Architecture. Carry Look Ahead adders, Carry Save adder, Pipelined array multiplier, Pipelined adder.

3.Control unit Design:

i) Design of a Processor ii) Control unit Design: Hardwired Control Unit, Microprogram Controlled Unit, Nano Program Control Unit.

MODULE2:

1 .ARM Cortex-M3 Processor:

i)Applications, Programming model – Register s, Operation modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces

ii) Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor and Pending Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.

iii)LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT

iv) to develop small applications by utilizing the ARM processor/LPC 17xx microcontroller.

MODULE 3:

the concept of RISC & CISC processors, limitations of Von-Neumann Architecture ,Harvard Architecture and VLIW Architecture,

MODULE4:

i)Programmable DSP (P-DSP) Processors:

Introduction to the computational requirements of DSP algorithms, architectural structure of DSP Processors: Pipelining, need of Harvard architecture in building DSP Processors, Multiple memory units, MAC unit, circular addressing scheme, zero overhead looping, bit reversal technique, butterfly computing unit, Barrel shifters,

ii)Introduction to TI DSP processor family:

Architectural details of TMS320C67xx series DSP Processors, data paths, cross paths, Introduction to Instruction level architecture of C54xx family, Assembly Instructions, memory addressing, for arithmetic, logical operations.

MODULE5:

DSP software development platform: Code Composer Studio for application development On chip peripherals, Processor benchmarking

Text Books:

1. Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 2ndEdition
2. John Hayes, "Computer Architecture and Organization", McGraw Hill Publications.
3. Venkatramani B. and Bhaskar M. "Digital Signal Processors: Architecture,Programming and Applications", TMH ,2ndEdition.
4. RulphChassaing, Donald Reay," Digital Signal Processing and Applications with the TMS320C6713 and TMS 320C6416 DSK", Willey Student Edition.

References:

5. SlossAndrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide: Designing and Optimizing", Morgan KaufmanPublication.
6. Steve furber, "ARM System-on-Chip Architecture", PearsonEducation
7. Frank Vahid and Tony Givargis, 'Embedded System Design",Wiley
8. Technical references and user manuals on www.arm.com,NXP Semiconductor www.nxp.comand Texas Instrumentswww.ti.com
9. Amitabha Sinha , " DSP – Algorithms, Architecture & Applications", MAKAUT

PGVES-103A : Elective I : Digital Signal and Image Processing
[Sem – I] 3(L) (36 Lectures) CREDIT-3

Teaching Scheme
Lectures: 3hrs/week

Course Outcomes:

At the end of this course, students will be able to

CO1: analyze discrete-time signals and systems in various domains
CO2: design and implement Digital Filters (FIR, IIR) using fixed and floating point Arithmetic on targeted platforms.
CO3: learn various transform algorithms for image coding and compression.
CO4: design, implement, compare and analyze computational complexities of different color Image Processing algorithms and to handle challenges.

CO5: learn architecture of different DSP Processors (16 bit/32-bit processors from TI, analog Devices) and VLSI architectures for implementation of Signal and Image Processing algorithms.

Syllabus Contents:

MODULE 1: Review of Discrete Time signals and systems, Characterization in time and frequency, Z transform, Fourier Transform: Discrete time FT, DFT, FFT algorithms – In place computations, Butterfly computations, bit reversal technique.

MODULE 2: Digital Filter design: FIR- Windowing and Frequency Sampling, IIR– Impulse invariance, bilinear transformation, fixed and floating-point implementation, challenges And techniques.

MODULE 3: Digital Image Acquisition, Enhancement, Restoration. Digital Image Coding and Compression– Cosine Transform, Wavelet Transform, JPEG and JPEG 2000.

MODULE 4: Detailed about Color Image processing – Handling multiple planes, computational challenges, different algorithms and detailed analysis of computational complexities .

MODULE 5: Hardware Platforms for implementing signal Processing Algorithms: DSP Processors (16 bit/32 bit from TI, analog Devices) , FPGAs and VLSI architectures for implementation of Signal and Image Processing algorithms, Pipelining , SIMD and Systolic architecture

Text Books:

1. J.G.Proakis,Manolakis"DigitalSignalProcessing",Pearson,4thEdition
2. GonzalezandWoods,"DigitalImageProcessing",PHI,3rdEdition
3. S.K.Mitra."DigitalSignalProcessing–AComputerbasedApproach",TMH,3rdEdition,2006
4. A.K.Jain,"Fundamentals of Digital Image Processing",PrenticeHall

References:

1.KeshabParhi,"VLSIDigitalSignalProcessingSystems– Design and Implementation",WileyIndia

2.Theory and Problems of Digital Signal Processing- M.H. Hayes (Tata Mcgraw- Hill Publishing Co.)

3.. Digital Signal Processing- Steve White (Cengage Learning,India edition)

4.Chassing, Donald Reay,".Digital Signal Processing & Applications with the TMS320C6713 and TMS320C6416" ,DSK – R. (Willey student edition)

5.www.ti.com , www.analogdevices.com , www.xilinx.com

6.. Amitabha Sinha," Lecture notes on Digital Signal Processing" ,MAKAUT

7. S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing,Prentice Hall, 1985.

8.www.cs.berkeley.edu/~pattrsn/152F97/slides/CS152_dsp.pdf

9.Bob Brodersen, "Introduction to Architectures for Digital Signal Processing" (http://infopad.eecs.berkeley.edu)

10. Mike Schulte," Application-Specific Processor Design", http://www.eecs.lehigh.edu/~mschulte/ece450-00

11.Uwe Meyer-Baese ," Digital Signal Processing with Field Programmable Gate Arrays", Springer, third edition

PGVES-103B : Elective I : Programming Languages for Embedded Software
[Sem – I] 3(L) (36 Lectures) CREDIT-3

Teaching Scheme Lectures: 3hrs/week

Course Outcomes:

At the end of this course, students will be able to

- Write an embedded C application of moderate complexity.
- Develop and analyze algorithms inC++.
- Differentiate interpreted languages from compiled languages.

Syllabus Contents:

MODULE 1:: Embedded 'C' Programming
Bitwise operations, Dynamic memory allocation, OS services Linked stack and queue, Sparse matrices, Binary tree Interrupt handling in C, Code optimization issues Writing LCD drives, LED drivers, Drivers for serial port communication Embedded Software Development Cycle Methods (Waterfall,Agile)

MODULE 2: Object Oriented Programming
Introduction to procedural, modular, object-oriented and generic programming techniques, Limitations of procedural programming, objects, classes, data members, methods, data encapsulation, data abstraction and information hiding, inheritance, polymorphism

MODULE 3:CPP Programming: 'cin', 'cout', formatting and 110 manipulators, new and delete operators, Defining a class, data members and methods, 'this' pointer, constructors, destructors, friend function, dynamic memory allocation

MODULE 4: Overloa ding and Inheritance: Need of operator overloading, overloading the assignment, overloading using friends, type conversions, single inheritance, base and derived classes, friend classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, polymorphism, virtual functions,

MODULE 5: Templates: Function template and class template, member function templates and template arguments, Exception Handling: syntax for exception handling code: try-catch-throw, Multiple Exceptions .

MODULE 6: Scripting Languages
Overview of Scripting Languages -PERL, CGI, VB Script, Java Script, PERL: Operators, Case study: Python for Embedded system development, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables, Inter process Communication Threads, Compilation &Line Interfacing.

References:

- Michael J.Pont , "Embedded C", Pearson Education, 2nd Edition,2008
- Randal L. Schwartz, "Learning Perl", O'Reilly Publications, 6th Edition,2011
- A. Michael Berman, "Data structures via C++", Oxford University Press,2002
- Robert Sedgewick, "Algorithms in C++", Addison Wesley Publishing Company,1999
- Abraham Silberschatz, Peter B, Greg Gagne, "Operating System Concepts",JohnWilley & Sons, 2005

PGVES-103C : Elective I : VLSI Signal Processing
[Sem – I] 3(L) (36 Lectures) CREDIT-3

Teaching Scheme
Lectures: 3hrs/week

Course Outcomes:

At the end of this course, students will be able to

CO1: acquire knowledge about DSP algorithms, its DFG representation, pipelining and parallel processing approaches.

CO2: acquire knowledge about retiming techniques, folding and register minimization path problems.

CO3: Ability to have knowledge about algorithmic strength reduction techniques and parallel processing of FIR and IIR digital filters.

CO4: acquire knowledge about finite word-length effects and round off noise computation in DSP systems.

Syllabus Contents:

Module1:Introduction to DSP systems, Pipelined and parallel processing.

Module 2:Iteration Bound, Retiming, unfolding, algorithmic strength reduction in filters and Transforms.

Module 3:Systolic architecture design, fast convolution, pipelined and parallel recursive and adaptive filters, Scaling and round off noise.

Module 4: Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic.

Module 5:Numerical strength reduction, synchronous, wave and asynchronous pipe lines, low power design.

Module6:Programmable digital signal processors: Computational requirements of DSP processor and Architecture , case studies : TI TMS320c6000 series DSP processor.

Text Books:

1.Keshab K. Parthi[A1], VLSI Digital signal processing systems, design and implementation [A2] , Wiley, Inter Science,1999.

2.Mohammad Isamail and Terri Fiez ,"Analog VLSI signal and information processing" , McGraw Hill,1994

3.S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, Prentice Hall, 1985.

References:

4.www.cs.berkeley.edu/~pattrsn/152F97/slides/CS152_dsp.pdf

5. Bob Brodersen, "Introduction to Architectures for Digital Signal Processing" (http://infopad.eecs.berkeley.edu)

6. Mike Schulte," Application-Specific Processor Design", http://www.eecs.lehigh.edu/~mschulte/ece450-00

7.Uwe Meyer-Baese ," Digital Signal Processing with Field Programmable Gate Arrays", Springer, third edition.

8. www.ti.com , www.analog.com, www.xilinx.com

PGVES-104A : Elective II : Parallel Architecture & Processing

PGVES-104 Parallel Architecture and Processing	**Lecture/Week:3 ,Total Lectures :36 Hrs**	**Credit:3**

Course Outcomes:
At the end of this course, students will be able to
CO1: Identify limitations of different architectures of Von-Neumann Architecture and learn different types of parallel architecture.
CO2: Learn the concept of Pipelining and different Pipelined Architecture for VLSI implementation.
CO3: Learn Super Scalar, VLIW and multithreaded Architecture.
CO4: To learn the concept of Data Flow Architecture-a non-Von Neumann architecture for performance enhancement.
CO5: Learn the concept of Programmable hardware and Reconfigurable Architecture.
CO6: Investigate issues related to Software (Parallel Programming Languages and techniques Operating Systems

Syllabus Contents:

MODULE 1: Overview of Parallel Processing, Flynn's classification, Performance analysis, Scalability, Concept of SIMD, MIMD and pipelining Architecture, Interconnection Network (Static & Dynamic), Shared Memory MIMD and distributed multiprocessor. Coarse grained and fine-grained multiprocessor

MODULE 2: Principles and implementation of Pipelining, Classification of pipelining processors, Advanced pipelining techniques, Processor level and Instruction level and Programming level pipelining, Static and Dynamic pipelining, Reservation table, Concept of Vector and Array Processing, Systolic Architecture, VLSI Array Processors.

MODULE3: Concept of Super Scalar Architecture, VLIW processors, Case study: TI TMS 320C54X , Pentium Processor, RISC V Processor, SPARC, Intel Itanium Processor, ,
Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions.

MODULE 4: Non-Von Neumann Architecture, Concept of Data Flow Computing, Data flow diagram, Data Flow graph as Parallel Programming Language, Static and Dynamic Data Flow machines, Tagged Token Data Flow Machine, Parallel Implementation of Computational functions and "If then else "clause on Data Flow Machine, Case studies: MIT Data Flow Project, Manchester Data Flow Architecture.

MODULE 5: Programmable Hardware and Architectural concept of FPGA, FPGA Programming , Reconfigurable Computing using FPGA as basic building block, Implementation of Parallel Architecture using FPGA(s) , Case studies : Implementation of RISC Processor and Parallel Architecture for FFT algorithms on FPGA.

MODULE 6: Parallel Programming Languages, Techniques: Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues, introduction to Operating systems for Parallel Processing.

Text Books:
1.KaiHwang,FayeA.Briggs,"ComputerArchitectureandParallelProcessing",MGHInternational Edition
2.KaiHwang,"AdvancedComputerArchitecture",TMH

3.V.Rajaraman,L.SivaramMurthy,"ParallelComputers",PHI.

4. William Stallings,"Architecture, Designing for performance"PrenticeHall, Sixth edition

References:

- H.T. Kung KaiHwang,ZhiweiXu,"Scalable Parallel Computing",MGH
- David Harris and Sarah Harris, "Digital Design and Computer Architecture", MorganKaufmann.
- Arvind, David E. Culler, "Data Flow Architecture", MIT/LCS/TM-294, 12 Feb.,1986 ,MIT,Massatusets.
- Dezso Sima, Terrence Fountain and Peter Kacsuk ," Advanced Computer Architecture" ,Pearson education,2007
- H.T .Kung ," Let's Design VLSI Algorithms", IEEE Computers, 1979
- www.ti.com
- www.xilinx.com
- Amitabha Sinha ," Lecture Notes on Parallel Architecture",MAKAUT

PGVES-104B : Elective II : System Design with Embedded Linux
[Sem – I] 3(L) (36 Lectures) CREDIT-3

Teaching Scheme
Lectures: 3 hrs/week

Course Outcomes:

At the end of this course, students will be able to

1. Familiarity of the embedded Linux development model.
2. Write, debug, and profile applications and drivers in embedded Linux.
3. Understand and create Linux BSP for a hardware platform

Syllabus Contents:

Unit I : Embedded Linux Vs Desktop Linux, Embedded Linux Distributions

Unit 2 : Embedded Linux
Architecture, Kernel Architecture -HAL, Memory manager, Scheduler, File System, I/O and Networking subsystem, IPC, User space, Start-up sequence

Unit 3 : Board Support Package
Embedded Storage: MTD, Architecture, Drivers, Embedded File System Embedded Drivers: Serial, Ethernet, I2c, USB, Timer, Kernel Modules

Unit 4 : Porting Applications
Real-Time Linux: Linux and Real time, Programming, Hard Real-time Linux

Unit 5 : Building and Debugging: Kernel, Root file system Embedded Graphics

Unit 6 : Case study of uClinux

References:

- Karim Yaghmour, "Building Embededd Linux Systems", O'Reilly &Associates
- P Raghvan, Amol Lad, SriramNeelakandan, "Embedded Linux System Design and Development", AuerbachPublications
- Christopher Hallinan, "Embedded Linux Primer: A Practical Real World Approach", Prentice Hall, 2nd Edition,2010.
- Derek Molloy, "Exploring BeagleBone: Tools and Techniques for Building with Embedded Linux", Wiley, 1st Edition,2014.

PGVES-104C : Elective II : CAD of Digital System
[Sem – I] 3(L) (36 Lectures) CREDIT-3

Teaching Scheme
Lectures:3 hrs/week

Course Outcomes:

At the end of this course, students will be able to

- Fundamentals of CAD tools for modelling, design, test and verification of VLSI systems.
- Study of various phases of CAD, including simulation, physical design, test and verification.
- Demonstrate knowledge of computational algorithms and tools for CAD.

Syllabus Contents:

Unit 1 : Introduction to VLSI Methodologies - Design and Fabrication of VLSI Devices, Fabrication Process and its impact on Design.

Unit 2 : VLSI design automation tools – Data structures and basic algorithms, graph theory and computational complexity, tractable and intractable problems.

Unit 3 : General purpose methods for combinational optimization - partitioning , floor planning and pin assignment, placement , routing.

Unit 4 : Simulation - logic synthesis, verification, high level Synthesis.

Unit 5 and 6 : MCMS-VHDL-Verilog-implementation of simple circuits using VHDL

References:

- N .A. Sherwani, "Algorithms for VLSI Physical Design Automation".
- S.H. Gerez, "Algorithms for VLSI Design Automation.

PGVES-191: Digital VLSI Lab [Sem – I] 4(P) (48 Practical Hours)
CREDIT-2

Teaching Scheme
Lectures : 4 hrs/week

Course Outcomes:

After the completion of this lab course students will be able to:

CO1 be familiarized with the steps by step process involved in VLSI design and with different EDA tools (open s as well as commercial)

CO2 write program in hardware description language (HDL) like Verilog, VHDL for digital circuits and learn de verification using test bench.

CO3 develop skill to design, simulate, synthesize and validate digital circuits on FPGA Platform using design To like Xilinx ISE / Icarus Verilog.

CO4. develop skill to design digital circuits using VLSI design Tools like DSCH & Microwind.

CO5.Develop the skill for Layout of digital circuit using EDA tools like Cadence and Electric.

Pre-requisite: Knowledge of high-level structured programming Language (preferably 'C' and /or digital Digital electronics.

Software & Hardware Tools –

Sl. No	Software Name / Hardware	Open Source / Purchase
1.	Xilinx ISE with iSim Simulator	Open Source Software
2.	Icarus Verilog with GTK Wave	Open Source Software
3.	DSCH and Microwind	Open Source Software
4.	Electric with LT Spice	Open Source Software
5.	FPGA Kit (Hardware)	Commercial
6.	Cadence EDA Software	Commercial

Part-A : FPGA Based Digital Design, synthesis and Validation

LAB – 1A: Introduction to FPGA Based Digital Design:
- Register-transfer-level abstraction
- Introduction to HDL Coding by Basic Digital Gates, Concept of Test Benches.
- Using Xilinx ISE Pack for HDL Coding, Simulation & Synthesis

LAB – 1B: Understanding the FPGA Board
- Identifying the Board Parts
- Procedure of Bit-Stream Downloading by Basic Digital Gates
- JTAG

LAB – 2: Writing HDL(Verilog, VHDL) Code, Test Bench for Simulation & Synthesis
- Combinational Circuit – Multiplexer, Demultiplexer, Decoder, Encoder,Half Adder, Full Adder Subtractor, Full Subtractor, Adder- Subtractor.
- Combinational Circuit – Ripple Carry, Carry look ahead adder
- Construction of Higher Level Multiplexer using Lower Level Multiplexer
- Circuit Designing using universal logic: Multiplexer

LAB – 3: Writing HDL (Verilog, VHDL) Code, Test Bench for Simulation & Synthesis
- Sequential Circuit –
- Flip-Flop – SR, D, JK, T
- Counter – Up, Down, Bidirectional, Ring, Ripple, Johnson, Mod-N.
- Register – Left/Right Shift Register, Construction of Memory.
- FSM – Mealy & Moore

LAB – 4: Writing Verilog Code, Test Bench for Simulation & Synthesis
1. ALU Design 2. A 12-bit CPU Design 3.FFT Processor Design

Part-B : Lab assignments with VLSI Design Automation tool (Cadence , DSCH and Microwind) for Layout Design.

LAB – 5: Lab assignments with Cadence , DSCH , Microwind:
- Familiar with VLSI Design Tools like:**Cadence, DSCH , Microwind**.
- Study and Validation of the behavior of the basic logic Gates on DSCH schematic window and Extra layouts using Microwind.
- Study and Validation of the behavior of Combinational logics a) Full adder using half adder, b)full sub using half subtractor c) Binary adder sub tractor circuit and d) Ripple carry adder circuit on DSCH sch window and Extract the layout using Microwind.

LAB – 6: Lab assignments with Cadence and Micro wind:
- Study and Validation of the behavior of a) Parity checker circuit, b) 2:4 decoder circuit, c) the 4:1 mu 2:1 mux circuit and d) 1 bit comparator circuit on DSCH schematic window and Extract the layou Microwind.
- Study and Validation of the behavior of 2:1 mux as a universal logic on DSCH schematic window and their layouts using Microwind.

LAB – 7: Lab assignments with DSCH and Microwind:
- Study and Validation of the behavior of Sequential logics a) Flip-flops: S-R, D, J-K, T b)Register c) C Ripple, Ring, Up, Down, Mod-N Counter circuit on DSCH schematic window and Extract the layou Microwind.

LAB – 8: Lab assignments with DSCH and Microwind:

- Study and Validation of the behavior of a) CMOS inverter circuit and b) CMOS- NOR circuit c) CMO circuit and d)CMOS Combinational circuit on DSCH schematic window and Extract the layout Microwind.

Part-C : Lab assignments with Cadence, Electric

LAB – 9: Lab Assignments with Cadence, Electric:

- Familiar with Schematic design and test using Electric.
- Study and Validation of the behavior of the basic Gates on Electric schematic window and Extract their using Electric.
- Study and Validation of combinational logic such as a) full adder using half adder, b) Full subtractor cir Ripple carry adder circuit, d) Binary adder subtractor circuit and e) Parity checker circuit and Extract the using Cadence, Electric.

LAB – 10: Lab Assignments with Cadence, Electric:

- Study and Validation of a) 2:4 decoder circuit and b) 4:1 mux using 2:1 mux circuit, c) 1 bit comparator and Extract the layout using electric.
- Study and Validation of the behavior of 2:1 mux as a universal logic and extract the layout using Ca Electric.

LAB – 11: Lab Assignments with Cadence, Electric:

- Study and Validation of Sequential logics a) Flip-flops: S-R, D, J-K, T b)Register c) Counter and Extr layout using electric
- Learn to design and Test of a) CMOS inverter b) CMOS-NAND, c) CMOS-XOR and CMOS Combin circuit and Extract the layout using Cadence, Electric.

Text Books:

1. Advanced Digital Design using Verilog-HDL , Michael. D. Ciletti, PHI publications.
2.Carver Mead, Lynn Conway, Introduction to VLSI Systems",B.S. Publication
3.John P Uyemura ," Chip Design for Submicron VLSI",Thompson Publication.
4. Etienne Scard., Sonia Delmas Bendhia ," Advanced CMOS cell Design :",McGraw Hill Professional
.

References:

1.K.V.K.K.Prasad ,Kattula Shyamala, "VLSI Design Black Book", dreamtech Publication
2.Baker,Li,Boyce,"CMOSCircuitDesign,Layout,andSimulation",Wiley,2nd Edition1. 3.Amitabha Sinha, "Lecture Notes on VLSI Design", MAKAUT

PGVES-192 : Microcontrollers and Programmable Digital Signal Processors Lab [Sem – I]
4(P) (48 Practical Hours) CREDIT-2

Teaching Scheme
Lectures: 4 hrs/week

Course Outcomes:

At the end of the laboratory work, students will be able to:

1. Install, configure and utilize tool sets for developing applications based on ARM processor core SoC and DSP processor.
2. Develop prototype codes using commonly available on and off chip peripherals on the Cortex M3 and DSP development boards.

List of Assignments:

A) Experiments to be carried out on Cortex-M3 development boards and using GNU tool-chain

1. Blink an LED with software delay, delay generated using the SysTicktimer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method , by interrupt method and flash the LED once every five switch presses.
5. UART Echo Test.
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGBLED.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case something goes wrong.
11. Sample sound using a microphone and display sound levels on LEDs.

B) Experiment s to be carried out on DSP C6713 evaluation kits and using Code Composer Studio(CCS)

1. To develop an assembly code and C code to compute Euclidian distance between any two points
2. To develop assembly code and study the impact of parallel, serial and mixed execution
3. To develop assembly and C code for implementation of convolution operation
4. To design and implement filters in C to enhance the features of given input sequence/signal

PGVES-105: Research Methodology and IPR
[Sem – I] 2(L) (25 Lectures) CREDIT-2

Teaching Scheme Lectures: l hrs/week

Course Outcomes:

At the end of this course, students will be able to

- Understand research problem formulation.
- Analyze research related information
- Follow research ethics
- Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
- Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
- Understand that IPR protection provides an incentive to inventors for further research work and investment in R &D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

Syllabus Contents:

Unit 1: Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem.

Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

Unit 2: Effective literature studies approaches, analysis Plagiarism, Research ethics,

Unit 3: Effective technical writing, how to write report, Paper; Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

Unit 4: Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

Unit 5: Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

Unit 6: New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

References :

- Stuart Melville and Wayne Goddard , "Research methodology: an introduction for science & engineering students"'
- Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"
- Ranjit Kumar, 2nd Edition , "Research Methodology: A Step by Step Guide for beginners"
- Halbert, "Resisting Intellectual Property", Taylor &Francis Ltd,2007.
- Mayall, "Industrial Design", McGraw Hill,1992.
- Niebel, "Product Design", McGraw Hill,1974.
- Asimov, "Introduction to Design", Prentice Hall,1962.
- Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New Technological Age",2016.
- T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand,2008

PGVES-106 : Audit I : English for Research Paper Writing [Sem – I] 2(L) (25 Lectures) CREDIT-0

Course objectives:

Students will be able to:

- Understand that how to improve your writing skills and level of readability
- Learn about what to write in each section
- Understand the skills needed when writing a Title Ensure the good quality of paper at very first-time submission

Syllabus

Units	CONTENTS	Hours

1	Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity	4
2	Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism,	4
3	Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.	4
4	key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the	4
5	skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions	4
6	useful phrases, how to ensure paper is as good as it could possibly be the first- time submission	4

SuggestedStudies:

1. Goldbort R (2006) Witting for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highm a n 'sbook.
4. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London , 2011

PGVES-106 : Audit I : Disaster Management
[Sem – I] 2(L) (25 Lectures) CREDIT-0

Course Objectives:

Students will be able to:

1. learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
2. critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
3. develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
4. critically understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countries they work in

Syllabus

Units	CONTEN TS	Hours
1	**Introduction** Disaster: Definition, Factors And Significance; Difference Between Hazard And Disaster; Natural And Manmade Disasters: Difference, Nature, Types And Magnitude.	4

2	**Repercussions Of Disasters And Hazards**: Economic Damage, Loss Of Human And Animal Life, Destruct ion Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.	4
3	**Disaster Prone Areas in India** Study Of Seismic Zones; Areas Prone To Floods And Droughts, Landslides And Avalanches; Areas Prone To Cyclonic And Coastal Hazards With Special Reference To Tsunami ; Post-Disaster Diseases And Epidemics	4
4	**Disaster Preparedness And Management** Preparedness: Monitoring Of Phenomena Triggering A Disaster Or Hazard; Evaluation Of Risk: Application Of Remote Sensing, Data From Meteorological And Other Agencies, Media Reports: Governmental And Community Preparedness.	4
5	**Risk Assessment** Disaster Risk: Concept And Elements, Disaster Risk Reduction, Global And National Disaster Risk Situation. Techniques Of Risk Assessment, Global Co-Operation In Risk Assessment And Warning, People's Participation In Risk Assessment. Strategies for Survival.	4
6	**Disaster Mitigation** Meaning, Concept And Strategies Of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation And Non-Structural Mitigation, Programs Of Disaster Mitigation In India.	4

SUGGESTED READINGS:

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'NewRoyal bookCompany.
2. Sahni, Pardeep Et.AL (Eds.)," Disaster Mitigation Experience s And Reflections", Prentice Hall Of India, NewDelhi.
3. Goel S. L. , Disaster Administration And Management Text And Case Studies" ,Deep &DeepPublication Pvt. Ltd., NewDelhi.

PGVES-106 : Audit I : Sanskrit for Technical Knowledge
[Sem – I] 2(L) (25 Lectures) CREDIT-0

Course Objectives

1. To get a working knowledge in illustrious Sanskrit, the scientific language in the world
2. Learning of Sanskrit to improve brain functioning
3. Learning of Sanskrit to develop the logic in mathematics, science &other subjects enhancing the memory power
4. The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from ancient literature

Syllabus

Unit	Content	Hours
1	• Alphabets in Sanskrit, • Past/Present/Future Tense, • Simple Sentences	8
2	• Order • Introduction of roots • Technical information about Sanskrit Literature	8
3	• Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics	8

Suggested reading

1. "Abhyaspustakam"- Dr. Vishwas , Samskrita-Bh arti Publication,New Delhi
2. "Teach Yourself Sanskrit" Prathama Deeksha-Vempati Kutumbshastri, Rashtriya SanskritSansthanarn, New DelhiPublication
3. "India 's Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., NewDelhi.

Course Output

Students will be able to

1. Understanding basic Sanskritlanguage
2. Ancient Sanskrit literature about science & technology can beunderstood
3. Being a logical language will help to develop logic instudents

PGVES-106 : Audit I : Value Education
[Sem – I] 2(L) (25 Lectures) CREDIT-0

Course Objectives

Students will be able to

1. Understand value of education and self-development
2. Imbibe good values in students
3. Let the should know about the importance of character

Syllabus

Unit	Content	Hours
1	• Values and self-development -Social values and individual attitudes. Work ethics, Indian vision of humanism. • Moral and non- moral valuation. Standards and principles. • Value judgments	4
2	• Importance of cultivation of values. • Sense of duty, Devotion, Self-reliance. Confidence, Concentration . Truthfulness, Cleanliness. • Honesty, Humanity. Power of faith, National Unity. • Patriotism. Love for nature, Discipline	6

3	• Personality and Behavior Development - Soul andScientific attitude. Positive Thinking. Integrity and d iscipline. • Punctuality, Love andKindness. • Avoid faultThinking. • Free from anger, Dignity oflabour. • Universal brotherhood and religioustolerance. • Truefriendship. • Happiness vs suffering, love fortruth. • Aware of self-destructivehabits. • Association and Cooperation. • Doing best for savingnature	6
4	• Character and Competence -Holy books vs Blind faith. • Self-management and Good health. • Science of reincarnation. • Equality, Nonviolence ,Humility, Role of Women. • All religions and same message. • Mind your Mind, Self-control. • Honesty, Studying effectively	6

Suggested reading

1. Chakroborty, S.K. "Values and Ethics for organizations Theory and practice", Oxford University Press, New Delhi

Course outcomes

Students will be able to

1. Knowledge of self-development
2. Leam the importance of Human values
3. Developing the overall personality

PGVES-106 : Audit I : Constitution of India
[Sem – I] 2(L) (25 Lectures) CREDIT-0

Course Objectives:

Students will be able to:

1. Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
2. To address the growth of Indian opm10n regarding modern Indian intellectuals ' constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
3. To address the role of socialism In India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.

Syllabus

Units	Content	Hour
1	•**History of Making of the Indian Constitution:** History Drafting Committee, (Composition & Working)	4
2	•**Philosophy of the Indian Constitution:** Preamble Salient Features	4

3	**•Contours of Constitutional Rights & Duties:** • Fundamental Rights • Right to Equality • Right to Freedom • Right against Exploitation • Right to Freedom of Religion • Cultural and Educational Rights • Right to Constitutional Remedies • Directive Principles of State Policy • Fundamental Duties.	4
4	**•Organs of Governance:** • Parliament • Composition • Qualifications and Disqualifications • Powers and Functions • Executive • President • Governor • Council ofMinisters • Judiciary, Appointm ent and Transfer of Judges,Qualifications • Powers andFunctions	4
5	**•LocalAdministration:** • District'sAdministrationhead:RoleandImportance, • Municipalities:Introduction, Mayor and role of Elected Representative, CEC of MunicipalCorporation. • Pachayatiraj:Introduction,PRI:ZilaPachayat. • Electedofficialsandtheirroles,CEOZilaPachayat:Positionandrole. • Blocklevel:OrganizationalHierarchy(Differentdepartments), • Villagelevel:RoleofElectedandAppointedofficials, • Importance of grass rootdemocracy	4
6	**•ElectionCommission:** • ElectionCommission:RoleandFunctioning. • Chief Election Commissioner and Election Commissioners. • StateElectionCommission:RoleandFunctioning. • InstituteandBodiesforthewelfareofSC/ST/OBCandwomen.	4

Suggested reading

1. TheConstitutionofIndia,1950(BareAct),GovernmentPublication.
2. Dr.S.N.Busi,Dr.B.R.AmbedkarframingofIndianConstitution,lstEdition,2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn.,Lexis Nexis, 2014.
4. D.D.Basu, IntroductiontotheConstitutionofIndia,LexisNexis,2015.

CourseOutcomes:

Students will be able to:

1. Discuss thegrowthof thedemandforcivilrightsinIndiafor thebulkofIndiansbefore thearrivalofGandhiinIndianpolitics.
2. Discuss the intellectualorigins of the framework of argument that informed theconceptualization of social reforms leading to revolution inIndia.
3. Discuss the circumstancessurrounding the foundation of the Congress Socialist Party[CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposalof direct elections through adult suffrage in the IndianConstitution.
4. Discuss the passage of the Hindu Code Bill of1956.

PGVES-106 : Audit I : Pedagogy Studies
[Sem – I] 2(L) (25 Lectures) CREDIT-0

Course Objectives:

Students will be able to:

4. Review existing evidence on the review topic to inform programme designand policy making undertaken by the DfID, other agencies andresearchers.
5. Identify critical evidence gaps to guide thedevelopment.

Syllabus

Units	Content	Hours
1	• Introduction andMethodology: • Aims and rationale, Policy background, Conceptual framework andterminology • Theories of learning, Curriculum , Teachereducation. • Conceptual framework, Researchquestions. • Overview of methodologv andSearching.	4
2	• Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developingcountries. • Curriculum,Teachereducation.	2
3	• Evidence on the effectiveness of pedagogicalpractices • Methodology for the in depth stage: quality a ssessment of included studies. • How can teacher education (curriculu m and practicum) and the school curricu lum and guidance materials best support effectivepedagogy? • Theory ofchange. • Strength and nature of the body of evidence for effectivepedagogicalpractices. • Pedagogic theory and pedagogicalapproaches. • Teachers'attitudesandbeliefsandPedagogicstrategies.	4
4	• Professional development: alignment with classroom practicesand follow-up support • Peersupport • Support from the head teacher and thecommunity. • Curriculum andassessment • Barriers to learning: limited resources and large cla sssizes	4
5	• Researchgapsandfuturedirections • Researchdesign • Contexts • Pedagogy • Teacher education • Curriculum andassessment • Dissemination and resea rchimpact.	2

Suggested reading

1. Ackers J,Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2):245-261.
2. Agrawal M (2004) Curricular reform in schools: The importa nce of evaluation, Journal ofCurriculum Stud ies, *36* (3):361-379.
3. AkyeampongK (2003) Teacher training in Ghana - does it count? Multi- si te teacher educat i on research project (MUSTER) country report 1. London : D FID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (20 13) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, *33* (3):272-282.
5. Alexander RJ (200 1) Culture and pedagogy: International comparisons in primary education.Oxford and Boston:Blach-well.
6. Chavan M (2003) Read India: A mass scale, rapid, 1earning to read'campaign.

7. www.pratham.org/images/resource%20working%20paper%202.pdf

Course Outcomes:

Students will be able to understand:

1. What pedagogical practices are being used by teachers in formal and informal classrooms in developingcountries?
2. What is the evidence on the effectiveness of these pedagogical practices, in what conditions, andwith what population oflearners?
3. How can teacher education (curriculum and practicum) and the school curriculum and guidancematerials best support effectivepedagogy?

PGVES-106 : Audit I : Stress Management by Yoga
[Sem – I] 2(L) (25 Lectures) CREDIT-0

Course Objectives

1. To achieve overall health of body andmind
2. To overcom estress

Syllabus

Unit	Content	Hours
1	• Definitions of Eight parts of yog. (Ashtanga)	8
2	• Yam and Niyam.Do's and Don't's inlife. i) Ahinsa, satva, astheva, Bramhacharva andaparigraha ii) Shaucha, santosh, tapa, swadhyav,Ishwarpranidhan	8
3	• Asan andPranayam i) Various yog poses and their benefits for mind &body ii) Regularization of breathing techniques and its effects-Types of pranayam	8

Suggested reading

1. 'Yogic Asanas for Group Tarining-Part- 1": Janardan Swami Yogabhyasi Mandal,Nagpur
2. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda , Advaita Ashrama (Publication Department) ,Kolkata

Course Outcomes

Students will be able to:

1. Develop healthy mind in a healthy body thus improving social healthalso
2. Improveefficiency

PGVES-106 : Audit I : Personality Development through Life Enlightenment Skills
[Sem – I] 2(L) (25 Lectures) CREDIT-0

Course Objectives

1. To learn to achieve the highest goalhappily
2. To become a person with stable mind, pleasing personality anddetermination

3. To awaken wisdom in student s

Syllabus

Unit	Content	Hours
1	Neetisatakam-Holistic development of personality • Verses- 19,20,2 1,22(wisdom) • Verses- 29,31,32 (pride &heroism) • Verses- 26,28,63,65(virtue) • Verses- 52,53,59 (dont's) • Verses- 71,73,75,78(do's)	8
2	• Approach to day to day work andduties. • Shrimad Bhagwad Geeta : Chapter 2-Verses 41,47,48, • Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23,35, • Chapter 18-Verses 45, 46,48.	8
3	• Statements of basicknowledge. • Shrimad Bhagwad Geeta: Chapter 2 - Verses 56, 62,68 • Chapter 12 - Verses 13, 14, 15, 16,17,18 • Personality of Role model. Shrimad Bhagwad Geeta:Chapter 2 - Verses 17, Chapter 3 - Verses36,37,42, • Chapter 4 - Verses 18,38,39 • Chapter 1 8 - Verses37,38,63	8

Suggested reading

1. "Srimad Bhagavad Gita" by Swami Swarupananda Advaita Ashram (Publication Department), Kolkata
2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P. Gopinath, Rashtriya Sanskrit Sansthanam, NewDelhi.

CourseOutcomes

Students will be able to

1. Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal inlife
2. The person who has studied Geeta will lead the nation and mankind to peace andprosperity
3. Study of Neetishatakam will help in developing versatile personality ofstudents.

Semester II

PGVES-201: Analog and Digital CMOS VLSI Design
[Sem – II] 3(L) (36 Lectures) CREDIT-3

Teaching Scheme
Lectures: 3 hrs/week

Course Outcomes:

At the end of this course, students will be able to:

- Analyze, design, optimize and simulate analog and digital circuits using CMOS constrained by the design metrics.
- Connect the individual gates to form the building blocks of a system.
- Use EDA tools like Cadence, Mentor Graphics and other open source software tools like Ngspice.

Syllabus Contents:

Technology Scaling and Road map, Scaling issues, Standard 4 mask NMOS Fabrication process.

Digital CMOS Design:

Unit I: Review: Basic MOS structure and its static behavior, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay, Stick diagram and Layout, Wire delay models. Inverter: Static CMOS inverter, Switching threshold and noise margin concepts and their evaluation, Dynamic behavior, Power consumption.

Unit 2: Physical design flow: Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic, ESD protection-human body model, Machine model.

Combinational logic: Static CMOS design, Logic effort, Ratioed logic, Pass transistor logic,

Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates, CMOS transmission gate logic.

Unit 3:Sequential logic: Static latches and registers, Bi-stability principle, MUX based latches, Static SR flip-flops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining, Pulse registers, Non-bistable sequential circuit.

Advanced technologies: Giga-scale dilemma, Short channel effects, High-k, Metal Gate Technology, Fin FET, TFET etc.

Analog CMOS Design:

Unit 4: Single Stage Amplifier: CS stage with resistance load, Divide connected load, Current source load, Triode load, CS stage with source degeneration. Source follower, Common-gate stage, Cascade stage, Choice of device models. Differential Amplifiers: Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbert cell.

Unit 5 :Passive and active current mirrors: Basic current mirrors, Cascade mirrors, Active current mirrors. Frequency response of CS stage: Source follower, Common gate stage, Cascade stage and difference pair, Noise

Unit 6: Operational amplifiers: One stage OPAMP, Two stage OPAMP, Gain boosting , Common mode feedback, Slew rate, PSRR, Compensation of 2 stage OPAMP, Other compensation techniques .

References:

- J P Rabaey, A P Chandrakasan. B Nikolic, "Digital Integrated circuits: A design perspective", Prentice Hall electronics and VLSI series, 2ndEdition.
- Baker, L Boyce, "CMOS Circuit Design. Layout, and Simulation", Wiley, 2ndEdition.
- Behzad Razavi , "Design of Analog CMOS Integrated Circuits", TMH,2007.
- Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford, 3rdEdition.
- R J Baker, "CMOS circuit Design. Layout and Simulation", IEEE Inc.,2008.
- Kang, S. and Leblebici, Y., "CMOS Digital IntegratedCircuits, Analysis and Design", TMH,3rdEdition.
- Pucknell, D.A. and Eshraghian. K.,'Basic VLSI Design", PHI, 3rdEdition.

PGVES-202: VLSI Design Verification and Testing [Sem – II]
3(L) (36 Lectures) CREDIT-3

Teaching Scheme
Lectures: 3 hrs/week

Course Outcomes:

At the end of this course, students will be able to:

- Familiarity of Front end design and verification techniques and create reusa ble test environments.
- Verify increasingly complex designs more efficiently andeffectively.
- Use EDA tools like Cadence, MentorGraphics.

Syllabus Contents:

Module 1: Basic concept of Testing &Verification and their differences, Automatic Testing equipment., testing in different stages of manufacturing, Design verification, chip yield, system level operation and testing, different testing algorithms,

Module 2:EDA tools for testing,Verification guidelines: Verification Process, Basic Testbench functionality, directed testing, Methodology basics, Constrained-Random stimulus, Functional coverage, Testbench components, Layered testbench, Building layered testbench, Simulation environment phases, Maximum code reuse, Testbench performance.

.**Module3:**Proceduralstatementsandroutines:tasks,functionsandvoidfunctions,Routinearguments,returningfromaroutine,Localdatastorage,TimevaluesConnectingthetestbenchanddesign:Separatingthetestbenchanddesign,Interfaceconstructs,Stimulustiming, Interface driving and sampling, Connecting it all together, Top-level scope Program – Module interactions.

Module4: Randomization, what to randomize, Randomization in System Verilog, Constraint details solution probabilities, controlling multiple constraint blocks, Valid constraints, In-line constraints, The pre-randomize and post-randomize functions,

Module 5:. Concept of Automatic Test pattern Generation (ATPG), Fault coverage, Fault models, Stuck-at -1, stuck-at-0 faults, transistor faults, collapsed faults, bridging faults, Delay Faults and Crosstalk, pattern sensitivity and coupling faults. Automatic Test Pattern Generation (ATPG): Algorithms for generating sequence of test vectors for a given circuit based on specific fault models, Fault analysis and Simulation to emulate fault models in CUT and application of test vectors to determine fault coverage: Parallel, deductive, and concurrent fault simulation, Design for testability, Scan, Built in self test ,Pseudo random number generator, Automatic Test Generation, Built in Logic Block observer (BILBO).

Module 6: Boundary Scan , JTAG (IEEE standard 1149.1) concept , Architecture and Instruction set and Boundary Scan TAP control operation ,testing process using JTAG(IEEE1149.4) for testing of Analog and Mixed signal VLSI circuits, Differences from digital testing , Test procedures, DSP based mixed signal test, Test plan , Boundary Scan Architecture & instruction Set of Mixed Signal Testing (IEEE1149.4) and test Process , Standard Analog Test Bus (ATB), Basic Mixed Signal Chip structure IEEE 1149. , Digital/Analog Interfaces ,Analog test access Port, Test Bus Interface circuit (TBIC),TBIC Switching Patterns, Chaining of 1149.4 compliance ICs.

Text Books:

1. N. K. Jha et.al.,"Testing of Digital Systems"
2. M L Bushnell and V D Agrawal. , "Essentials of Electronic Testing"
3. M Abramovici and A D Friedman. , " Digital Systems Testing and Testable Design"
4..M. L. Bushnell and V.D. Agrawal, Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits, Springer, 2005.
5. M. Abramovici, M. Breuer, and A. Friedman, *Digital System Testing and Testable Design*, IEEE Press, 1994

References:

1.ChrisSpears,"SystemVerilogforVerification", Springer,2nd Edition
2.M.BushnellandV.D. Agrawal,"EssentialsofElectronicTestingforDigital,MemoryandMixed-SignalVLSI Circuits", Kluwer Academic Publishers
3.IEEE 1800-2009 standard (IEEE Standard for System Verilog— Unified HardwareDesignSpecification, and Verification Language).
4. Amitabha Sinha, "Lecture notes on Testing & Verification of VLSI circuits", MAKAUT.
5. H. Fujiwara, *Logic Testing and Design for Testability*, MIT Press, 1985

PGVES-203A : Elective III : Memory Technologies
[Sem – II] 3(L) (36 Lectures) CREDIT-3

Teaching Scheme

Lectures: 3hrs/week

Course Outcomes:

At the end of the course, students will be able to:

- Select architecture and design semiconductor memory circuits and subsystems.
- Identify various fault models, modes and mechanisms in semiconductor memories and their testing procedures.
- Knowhow of the state-of-the-art memory chip design

Syllabus Contents:

Unit l:Random Access Memory Technologies:
Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Low Power RAMs, Advanced SRAM Architectures, Application Specific SRAMs.

Unit 2: DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs. SRAM and DRAM Memory controllers.

Unit 3: Non-Volatile Memories: Masked ROMs, PROMs, Bipolar &CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

Unit 4: Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing.

Unit 5:Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs),
Experimental Memory Devices.

Unit 6: Memory Hybrid s (2D &3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging

References:

- Ashok K Sharma, "Advanced Semiconductor Memories: Architectures, Designs and Applications", Wiley Interscience
- Kiyoo Itoh, "VLSI memory chip design", Springer International Edition
- Ashok K Sharma ," Semiconductor Memories: Technology, Testing and Reliability , PHI

PGVES-203B : Elective III : SoC Design
[Sem – II] 3(L) (36 Lectures) CREDIT-3

Teaching Scheme Lectures: 3 hrs/week

Course Outcomes:

At the end of the course, students will be able to:

- Identify and formulate a given problem in the framework of SoC based designapproaches
- Design SoC based system for engineeringapplications
- Realize impact of SoC on electronic design philosophy and Macro-electro nics thereby incline towards entrepreneurship &skilldevelopment.

Syllabus Contents:

Unitl:ASIC

Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.

Unit 2: NISC

- NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction• set Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embeddedprocessors.

Unit 3: Simulation

- Different simulation modes, behavioural functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA,Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree designissues.

Unit 4: Low power SoC design / Digital system,

- Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

Unit 5:Synthesis

- Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs

Unit 6:Case study for overview of cellular phone design with emphasis on area optimization, speed improvement and power minimization.

Note: Students will prepare and present a term paper on relevant identified current topics (in batches of three students per topic) as a part of theory course.

References:

- Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge Univer sity Press,2008.
- B. Al Hashimi, "System on chip-Next generation electronic s", The IET,2006
- RochitRajsuman, "System-on- a-chip: Design and test", Advantest America R &D Center,2000
- P Mishra and N Dutt, "Processor Description Language s", Morgan Kaufmann,2008
- Michael J. Flynn and Wayne Luk, "Computer System Design: System-on-Chip". Wiley,2011

PGVES-203C : Elective III : Low Power VLSI Design
[Sem – II] 3(L) (36 Lectures) CREDIT-3

Teaching Scheme Lectures: 3 hrs/week

Course Outcomes:

At the end of the course, students will be able to:

- CO 1: Identify the sources of power dissipation in digital IC systems &understand the impact of power on system performance and reliability.
- C02: Characterize and model power consumption & understand the basic analysis methods.
- C03: Understand leakage sources and reduction techniques

Syllabus Contents:

Unit 1: Technology & Circuit Design Levels: Sources of power dissipation in digital ICs, degree of freedom, recurring themes in low-power, emerging low power approaches, dynamic dissipation in CMOS, effects of Vdd & Vt on speed , constraints on Vt reduction, transistor sizing & optimal gate oxide thickness, impact of technology scaling, technology innovations.

Unit 2: Low Power Circuit Techniques: Power consumption in circuits, flip-flops &latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches.

Unit 3: Low Power Clock Distribution: Power dissipation in clock distribution, single driver vs. distributed buffers, buffers & device sizing under process variations, zero skew vs. tolerable skew, chip & package co-design of clock network.

Unit 4: Low power SoC design / Digital system,

- Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

Unit 5: Low Power Memory Design: Sources &reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM &SRAM, low power DRAM circuits, low power SRAM circuits.

Unit 6:Low Power Microprocessor Design System: power management support, architectural trade-offs for power, choosing the supply voltage, low-power clocking, implementation problem for low power, comparison of microprocessors for power &performance.

References:

- P. Rashinkar, Paterson and L. Singh, "Low Power Design Methodologies ",Kluwer Academic,2002
- Kaushik Roy, Sharat Prasad, "Low power CMOS VLSI circuit design", John Wileysonslnc.,2000.
- J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley,1999.
- A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design",Kluwer,1995

PGVES-204A : Elective IV : Communication Buses and Interfaces
[Sem – II] 3(L) (36 Lectures) CREDIT-3

Teaching Scheme
Lectures: 3 hrs/week

Course Outcomes:

At the end of the course, students will be able to:

- Select a particular serial bus suitable for a particular application.
- Develop APIs for configuration, reading and writing data onto serial bus.
- Design and develop peripherals that can be interfaced to desired serial bus.

Syllabus Contents:

Unit I: Serial Busses

- Physical interface, Data and Control signals, features,

Unit 2: limitations and applications of RS232, RS485, I^2C, SPI

Unit 3: CAN - Architecture, Data transmission, Layers, Frame formats, applications

Unit 4: PCIe - Revisions, Configuration space, Hardware protocols, applications

Unit 5:USB - Transfer types, enumeration, Descriptor types and contents, Device driver

Unit 6: Data Streaming Serial Communication Protocol

- Serial Front Panel Data Port (SFPDP) using fibre optic and copper cable

References:

- Jan Axelson, "Serial Port Complete - COM Ports, USB Virtual Com Ports, and Portsfor Embedded Systems ", Lakeview Research, 2nd Edition
- Jan Axelson, "USB Complete", PenramPublications
- Mike Jackson, Ravi Budruk, "PCI Express Technology", MindsharePress
- Wilfried Voss, "A Comprehensible Guide to Controller Area Network", Copperhill Media Corporation, 2nd Edition,2005.
- Serial Front Panel DraftStandard VITA 17.1 -200x
- Technical references onwww.can-cia.org,www.pcisig.com,www.usb.org

PGVES-204B : Elective IV : Introduction to AI , Machine Learning and Applications
[Sem – II] 3(L) (36 Lectures) CREDIT-3

Teaching Scheme
Lectures: 3 hrs/week

Course Outcomes:
CourseOutcomes:

At the end of the course, students will be able to:

CO1: Learn the basic concept of Artificial Intelligence, Machine Learning , Neural network and their inter-relations different AI techniques

CO2: Learn the concept of Knowledge Representation and knowledge representation issues and the concept of Logic programming.

CO3: Learn the concept of Reasoning under uncertainty for Artificial Intelligence

CO4: Learn the basic concept of Biological Network and modelling of Artificial Neural Network.

CO5: Learn the concept of Machine Learning and different types of Machine Learning Network

CO6: Learn the Architecture of Convolutional Neural Network (CNN) & it's application to Image classification and VLSI implementation of Machine Learning Engine.

SyllabusContents:

MODULE 1: Introduction to AI, Machine Learning, Deep Learning and Neural Network and their inter relation, Machine Learning vs Neural Network and key differences,

The AI Problems, The Underlying Assumption, AI Techniques, Level of The Model, Criteria For Success, Some General References, One Final Word Problems, State Space Search & Heuristic Search Techniques: Defining The Problems as aStateSpaceSearch,ProductionSystems,ProductionCharacteristics,ProductionSystemCharacteristics, Issues In The Design Of Search Programs, Additional Problems. Generate-And-Test, Hill Climbing, Best-First search and Breadth-first Search, \ Problem Reduction, Constraint Satisfaction, Means-Ends Analysis.

MODULE 2:

Knowledge Representation Issues: Representations And Mappings, Approaches To Knowledge Representation. Using Predicate Logic: Representation Simple Facts In Logic, Representing Instance And Isa Relationships, Computable Functions And Predicates, Resolution. Representing Knowledge Using Rules: Procedural Versus Declarative Knowledge ,Logic Programming, Forward Versus Backward Reasoning.

MODULE 3:

Symbolic Reasoning under uncertainty: Introduction To Nomonotonic Reasoning, Logics For Non-monotonic Reasoning. Statistical Reasoning: Probability And Bays 'Theorem, Certainty Factors And Rule-Base Systems, Bayesian Networks, Dempster Shafer Theory

MODULE4:

Concept and structure and functions of Biological Neuron, introduction to function of Human Brain, Characteristics of Biological Neural Network, Introduction to Artificial Neural Network (ANN), Non-Linear Characteristics, model of an Artificial Neural Network, Properties of ANN, Layers and structures of ANN, Forward and Back Propagation NN, Different Activation Functions,

MODULE 5:

Concept of Learning, Machine Learning and key elements, Different types of machine Learning:Supervised learning Unsupervised learning, Semi-supervised learning, Reinforcement learning, Adaptive Learning, Difference between traditional programming and machine Learning. Deep Learning Network, Concept of Convolution and Convolutional Neural Network (CNN), Layers of CNN: Pooling Layer, Max Pooling Layer, Global average Pooling Layer, Normalization Layer, Fully-Connected Layer , Converting Fully Connected Layers to Convolutional Layers, different Activation Layers.

MODULE 6:

Architecture of CNN: Layer Patterns ,Layer Sizing Patterns , Image Classification using CNN: CNN Architecture of Image Classification ,concept of activation Layer RELU ,Details about CNN, Stages of CNN, concepts of Filters, Stride, Padding, Filter hyperparameters, Parameter Sharing
Filter Activations: Feature maps, Soft Max Function, Computational considerations.
Efficient Hardware Realization for Neural Networkof CNN, Reconfigurable VLSI Architecture of CNN, Concept and need of Reconfigurability, VLSI AI Engines to Provide Compute Density for Machine Learning, Case studies (Xilinx AI engine), Concept of" Near Memory Computing" and Analog VLSI for implementing Machine Learning Systems, Neural Network training using Analog Memory, State-of-the-art Analog Deep Machine Learning Systems.

Text Books:

1.Elaine Rich and Kevin Knight "Artificial Intelligence", 2nd Edition, Tata McGraw-Hill, 2005.

2..

StuartRusselandPeterNorvig,"ArtificialIntelligence:AModernApproach",3rdEdition,PrenticeHall,2009

References:

1. Amitabha Sinha , " AI. Machine Learning & Applications in Image Classifications", MAKAUT
2. Jianxin Wu ,"Introduction to Convolutional Neural Networks", LAMDA Group National Key Lab for Novel Software Technology Nanjing University, China wujx2001@gmail.com May 1, 2017 (https://cs.nju.edu.cn/wujx/paper/CNN.pdf)
3.https://towardsdatascience.com/an-introduction-to-convolutional-neural-networks-eb0b60b58fd7
4.Himadri Sankar Chatterjee,"A Basic Introduction to Convolutional Neural Network",https://medium.com/@himadrisankarchatterjee/a-basic-introduction-to-convolutional-neural-network-8e39019b27c4

PGVES-204C : Elective IV : Physical Design Automation [Sem – II]
3(L) (36 Lectures) CREDIT-3

Teaching Scheme
Lectures: 3 hrs/week

Course Outcomes:

Course Outcomes:

At the end of this course, students will be able to

CO1: Study automation process for VLSI System design.
CO2: Understand different layout models
CO3: Understand different methods of global placement.
CO4: Learn minimization of timing-driven placement and global routing
CO5: Learn the concept of multi-layer routing.
CO6: Develop and enhance the existing algorithms and computational techniques For physical design process of VLSI systems

MODULE1:Introduction to VLSI Physical Design Automation.
MODULE2: Standard cell, Performance issues in circuit layout, delay models Layout styles.
MODULE3:Discrete methods in global placement.
MODULE4:Timing-drivenplacement.GlobalRoutingViaMinimization.
MODULE5: Over the Cell Routing - Single layer and two-layer routing, Clock and Power Routing.
MODULE6: Compaction, algorithms, Physical Design Automation of FPGAs.

Text Books:

1.N.A.Sherwani,"VLSIPhysicalDesignAutomation"., Springer
2. S.H.Gerez, "Algorithms for VLSI Design Automation, Wiley India (pdf free download
3. S.H.Gerez, "CAD For VLSI Algorithms For VLSI Design Automation", John Wiley & sons

References:

4. Jason Cong "VLSI Physical Design Automation", Computer Science Department , http://cadlab.cs.ucla.edu/~cong/cs258f_handouts.html
5. VLSI Physical Design Automation - VAST lab at UCLA, https://cadlab.cs.ucla.edu ›

PGVES-291: Analog VLSI Design Lab [Sem – II] 4(P) (48 Practical hours) CREDIT-2

Teaching Scheme
Lab work : 4 hrs/week

Course Outcomes:

After the completion of the course , students will be able to

CO1. be familiarized with VLSI Tool like cadence virtuoso.
CO2. design analog circuit using schematic editor window and also be able to test the design.
CO3. extract the Layout of analog circuits and CMOS circuits using Layout-XL.
CO4. Carry on transient, dc and ac analysis of the designed circuit using cadence virtuoso.
CO5. understand the DRC check, LVS and RC Extraction.
CO6. be familiarized with LTSpice Tool and design and test circuits..
CO7. Be familiarized with the concept of FPAA and implement different mathematical functions on FPAA platform.

List of Lab Assignments:

List of Lab assignments with LTSpice and cadence virtuoso:

1. i) Familiar with VLSI Design Tools like: LTSpice and cadence virtuoso.
ii) Design the schematic of an Inverter using **cadence virtuoso** and verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

2. Design and simulate the schematic of the common source amplifier. And verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

3. Design and simulate the schematic of the common drain amplifier, and perform the physical verification for the layout of the same. Verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

4. Design and simulate the schematic of a stage differential amplifier and perform the physical verification for the layout of the same. Verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

5. Design and simulate the schematic of the operational amplifier and perform the physical verification. Verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

6. Design and simulate the schematic of the cascode current mirror and perform the physical verification. Verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

7. Design and simulate the schematic of wilson current mirror and perform the physical verification. Verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

8. Implement i) adders/Subtractors, Multipliers, Differentiators, Integrators, ii) discrete analog filter using FPAA kit

References:

1.Razavi,B.,"DesignofAnalogCMOSIntegratedCircuits",1stEd.,McGraw

Hill.2001

2.Gray,P.R.,Hurst,P.J.,Lewis,S.H.,Meyer,R.G.,"AnalysisandDesign ofAnalog IntegratedCircuits",4thEd.,JohnWiley and Sons.2001

3..Ramon Pallas-Areny, John G.Webster, " Analog Signal Processing",Willey Student Edition.

4..AN231E04 Datasheet Rev 1.3

5.. A Programmable and Configurable Mixed-Mode FPAA SoC, Jennifer Hasler et al., Georgia Tech., January 7, 2016". doi:10.1109/TVLSI.2015.2504119.

6. David Johns and Ken Martin, "Switched -Capacitor Circuits", Lecture notes :University of Toronto, (johns@eecg.toronto.edu)/ (martin@eecg.toronto.edu).

7. Amitabha Sinha, "Lecture Notes on Switched Capacitor", MAKAUT

PGVES-292: VLSI Design Verification and Testing Lab
[Sem – II] 4(P) (48 Practical hours) CREDIT-2

Teaching Scheme
Lectures: 4 hrs/week

Course Outcomes:

At the end of the laboratory work, students will be able to:

- Verify increasingly complex designs more efficiently andeffectively.
- Use EDA tools like Cadence, MentorGraphics.

List of Assignments:

I. Sparse memory
2. Semaphore
3. Mailbox
4. Classes
5. Polymorphism
6. Coverage
7. Assertions

PGVES-281: Mini Project
[Sem – II] 4(P) (48 Practical hours) CREDIT-2

Teaching Scheme
Lab work : 20 and 32 hrs/week

Course Outcomes:

At the end of this course, students will be able to

- Ability to synthesize knowledge and skills previously gained and applied to an in- depth study and execution of new technical problem.
- Capable to select from different methodologies, methods and forms of analysis to produce a suitable research design, and justify their design.
- Ability to present the findings of their technical solution in a written report.
- Presenting the work in International/ National conference or reputed journals.

Syllabus Contents:

The dissertation / project topic should be selected/chosen to ensure the satisfaction of the urgent need to establish a direct link between education, national development and productivity and thus reduce the gap between the world of work and the world of study. The dissertation should have the following

- Relevance to social needs of society
- Relevance to value addition to existing facilities in the institute
- Relevance to industry need
- Problems of national importance
- Research and development in various domain The student

should complete the following:

- Literature survey Problem Definition
- Motivation for study and Objectives
- Preliminary design / feasibility / modular approaches
- Implementation and Verification
- Report and presentation

The dissertation stage II is based on a report prepared by the students on dissertation allotted to them. It may be based on:

- Experimental verification / Proof of concept.
- Design, fabrication, testing of Communication System.
- The viva-voce examination will be based on the above report and work.

PGVES-205 : Audit II : English for Research Paper Writing
[Sem – II] 2(L) (25 Lectures) CREDIT-0

Course objectives:

Students will be able to:

- Understand that how to improve your writing skills and level of readability
- Learn about what to write in each section
- Understand the skills needed when writing a Title Ensure the good quality of paper at very first-time submission

Syllabus:

Same as PGMSDVD-106 : Audit I : English for Research Paper Writing

PGVES-205 : Audit II : Disaster Management [Sem – II]
2(L) (25 Lectures) CREDIT-0

Course Objectives:

Students will be able to:

1. learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
2. critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
3. develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations. critically understand the strengths and weaknesses of disaster management approaches, planning andprogramming in different countries, particularly their home country or the countriesthey workin

Syllabus:

Same as PGMSDVD-106 : Audit I : Disaster Management

PGVES-205 : Audit II : Sanskrit for Technical Knowledge [Sem – II] 2(L)
(25 Lectures) CREDIT-0

CourseObjectives:

1. To get a working knowledge in illustrious Sanskrit, the scientific languagein the world
2. Learning of Sanskrit to improve brainfunctioning
3. Learning of Sanskrit to develop the logic in mathematics, science &other subjects enhancing the memorypower
4. The engineering scholars equipped with Sanskrit will be able to explore the hugeknowledge from ancientliterature

Syllabus:

Same as PGMSDVD-106 : Audit I : Sanskrit for Technical Knowledge

Course Outcome:

Students will be able to

1. Understanding basic Sanskritlanguage
2. Ancient Sanskrit literature about science & technology can beunderstood
3. Being a logical language will help to develop logic instudents

PGVES-205 : Audit II : ValueEducation
[Sem – II] 2(L) (25 Lectures)CREDIT-0

CourseObjectives:

Students will be able to

1. Understand value of education and self-development
2. Imbibe good values instudents
3. Let the should know about the importance ofcharacter

Syllabus:

Same as PGMSDVD-106 : Audit I : Value Education

Course Outcome:

Students will be able to

1. Knowledge ofself-development
2. Learn the importance of Humanvalues
3. Developing the overallpersonality

PGVES-205 : Audit II : Constitution of India [Sem – II]
2(L) (25 Lectures) CREDIT-0

CourseObjectives:

Students will be able to:

1. Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
2. To address the growth of Indian opm10nregarding modern Indian intelle ctua l s'constitutiona l role and entitlem ent to civil and economic right s as well as theemergence of nationhood in the early years of Indian nationalism.
3. To address the role of socialism In India after the comm encement of the Bolshev ikRevolution in 1917 and its impact on the init ia l drafting of the Indian Constitution.

Syllabus:

Same as PGMSDVD-106 : Audit I : Constitution of India

Course Outcomes:

Students will be able to:

1. DiscussthegrowthofthedemandforcivilrightsinIndiaforthebulkofIndiansbeforethearrivalof GandhiinIndianpolitics.
2. Disc uss the intellectua lorigins of the framework of argument that inform edthe conceptualizationof socia l reforms leading to revolution inIndia.
3. Discuss the circumstances surrounding the foundation of the Congress SocialistParty [CSP] under the leadership of Jawaharlal Nehru and the eventual failure oftheproposalofdirectelectionsthroughadultsuffrageintheIndianConstitution.
4. DiscussthepassageoftheHinduCodeBillof1956.

PGVES-205 : Audit II : Pedagogy Studies [Sem – II] 2(L)
(25 Lectures) CREDIT-0

CourseObjectives:

Students will be able to:

4. Review existing evidence on the review topic to inform programme design and policymakingundertakenbytheDfID,otheragenciesandresearchers.
5. Identify critica l evidence gaps to guide the development.

Syllabus:

Same as PGMSDVD-106 : Audit I : Pedagogy Studies

Course Outcomes:

Students will be able to understand:

1. What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries?
2. What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
3. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

PGVES-205 : Audit II : Stress Management by Yoga [Sem – II]
2(L) (25 Lectures) CREDIT-0

Course Objectives:

1. To achieve overall health of body and mind
2. To overcome stress

Syllabus:

Same as PGMSDVD-106 : Audit I : Stress Management by Yoga

Course Outcomes:

Students will be able to:

1. Develop healthy mind in a healthy body thus improving social health also
2. Improve efficiency

PGVES-205 : Audit II : Personality Development through Life Enlightenment Skills [Sem – II]
2(L) (25 Lectures) CREDIT-0

Course Objectives:

1. To learn to achieve the highest goal happily
2. To become a person with stable mind, pleasing personality and determination
3. To awaken wisdom in students

Syllabus:

Same as PGMSDVD-106 : Audit I : Personality Development through Life Enlightenment Skills

Course Outcomes:

Students will be able to

1. Study of Shrimad-Bhagwad- Geeta will help the student in developing his personality and achieve the highest goal inlife
2. The person who has studied Geeta will lead the nation and mankind to peace and prosperity
3. Study of Neetishatakam will help in developing versatile personality ofstudents.

Semester III

PGVES-301A: Elective V : Communication Network
[Sem – III] 3(L) (36 Lectures) CREDIT-3

Teaching Scheme
Lectures: 3 hrs/week

Course Outcomes:

At the end of the course, students will be able to:

- Analyze protocols and algorithms, acknowledge tradeoffs andrationale
- Use routing, transport protocols for the given networking scenario andapplication
- Evaluate and develop small networkapplications

Syllabus Contents:

Unit I: Introduction:
- Network Architecture,Performance

Unit 2: Connecting nodes:
- Connecting links, Encoding , framing, Reliable transmission, Ethernet and Multiple access networks, Wirelessnetworks

Unit 3: Queuing models
- For a) one or more servers b) with infinite and finite queue size c) Infinitepopulation

Internetworking:
- Switching and bridging, IPv4, Addressing, Routing Protocols, Scale issues,Routers - Architecture, IPv6

Unit 4: End-to-End Protocols:
- Services, Multiplexing , De-multiplexing, UDP, TCP, RPC,RTP

Unit 5: Congestion control and Resource Allocation
- Issues, Queuing disciplines , TCP congestion control, Congestion Avoidance, QoSApplications:
- Domain Name Resolution, File Transfer, Electronic Mail, WWW,Multimedia Applications

Unit 6: Network monitoring -Packet sniffing tools such as Wireshark Simulations using NS2/0PNET

References:

- Larry L. Peterson, Bruce S, Devie, "Computer Networks", MK, 5thEdition
- Aaron Kershenbaum, "Telecommunication Network Design Algorithms",MGH, International Edition1993.
- Vijay Ahuja, "Communications Network Design and Analysis of Computer Communication Networks", MGH, InternationalEditions.
- Douglas E. Comer, "Internetworking with TCP/IP", Pearson Education, 6th Edition

PGVES-301B: Elective V : Selected Topics in Mathematics
[Sem – III] 3(L) (36 Lectures) CREDIT-3

Teaching Scheme Lectures: 3 hrs/week

Course Outcomes:

At the end of the course, students will be able to:
- Characterize and represent data collected from experiments using statisticalmethods.
- Model physical process/systems with multiple variables towards parameter estimation andprediction
- Represent systems/architectures using graphs and trees towards optimizingdesired objective.

Syllabus Contents:

Please Add the following module in Math syllabus.

Module-1 :

Laplace Transform and solving differential equations and applications to electric circuit analysis.

Fourier series and Transform: Revision of Fourier series, integrals and transforms and their properties. The Two-dimensional Fourier transform, convolution theorem, Parseval's formula, discrete fourier transform, fast fourier transform.

Z-transforms: sequence, representation of sequence, basic operations on Sequences, z transforms, properties of z transforms, change on scale, shifting Property, inverse z transform, solution of difference equations, region of Convergence, bilinear (s to z) transform , difference among Laplace and Z transforms.

Walsh function and Hadamard transform: generating walsh functions of Order n, characteristics and applications

of walsh function, Hadamard Matrix, properties, fast Hadamard transform, applications

Module-2 : Probability and Statistics:

- Definitions, conditional probability, Bayes Theorem and independence.
- Random Variables: Discrete, continuous and mixed random variables, probability mass, probability density and cumulative distribution functions, mathematical expectation, moments, moment generating function, Chebyshevinequality.

Module-3 : Special Distributions: Discrete uniform, Binomial, Geometric, Poisson, Exponential, Gamma, Normal distributions.

– Pseudo random sequence generation with given distribution, Functions of a Random Variable

Module-4 : Joint Distributions: Joint, marginal and conditional distributions, product moments, correlation, independence of random variables, bi-variate normal distribution.

- Stochastic Processes: Definition and classification of stochastic processes, Poisson process
- Norms, Statistical methods for ranking data

Module-5 : Multivariate Data Analysis

- Linear and non-linear models, Regression, Prediction and Estimation
- Design of Experiments – factorial method
- Response surface method

Module-6: Graphs and Trees:

- Graphs: Basic terminology, multi graphs and weighted graphs, paths and circuits, shortest path Problems, Euler and Hamiltonian paths and circuits, factors of a graph, planar graph and Kuratowski's graph and theorem, independent sets, graphcolouring

Module-7 : Trees: Rooted trees, path length in rooted trees, binary search trees, spanning trees and cut set, theorems on spanning trees, cut sets , circuits, minimal spanning trees, Kruskal 's and Prim's

References:

- Henry Stark, John W. Woods, "Probability and Random Process with Applications to Signal Processing", Pearson Education, 3rdEdition
- C. L. Liu, "Elements of Discrete Mathematics", Tata McGraw-Hill, 2"dEdition
- Douglas C. Montgomery, E.A. Peck and G. G. Vining, "Introduction to Linear Regression Analysis", John Wiley and Sons,2001.
- Douglas C. Montgomery, 'Design and Analysis of Experiment s", John Wiley and Sons,2001.
- B. A. Ogunnaike, "Random Phenomena: Fundamentals of Probability and Statistics for Engineer s", CRC Press,2010.

PGVES-301C: Elective V : Nanomaterials and Nanotechnology
[Sem – III] 3(L) (36 Lectures) CREDIT-3

Teaching Scheme Lectures: 3 hrs/week

CourseOutcomes:

- At the end of the course, students will be ableto:

CO 1: To understand the basic science behind the design and fabrication of nano scale systems.

C02: To understand and formulate new engineering solutions for current problems and competing technologies for future applications.

C03: To be able make inter disciplinary projects applicable to wide areas by clearing and fixing the boundaries in system development.

C04: To gather detailed knowledge of the operation of fabrication and characterization devices to achieve precisely designed systems.

Syllabus Contents:

Unit l:Nanomaterials in one and higher dimensions,

Unit 2: Applications of one and higher dimension nano-materials.

Unit 3: Nano-lithography, micro electro-mechanical system (MEMS) and nano-photonics.

Unit 4: Multidimensional devices - synthesis and applications

Unit 5 and 6: Interdisciplinary arena of nanotechnology.

References:

- Nanoscale Materials in Chemistry edited by Kenneth J. Klabunde and Ryan M. Richards, 2"dedn, John Wiley and Sons,2009.
- Nanocrystalline Materials by A I Gusev and A ARempel, CambridgeInternational Science Publishing, 1st Indian edition by Viva Books Pvt. Ltd. 2008.
- Springer Handbook of Nanotechnology by Bharat Bhushan, Springer, 3rdedn,2010.
- Carbon Nanotubes: Synthesis, Characterization and Applications by KamalK. Kar, Research Publishing Services; lstedn, 2011, ISBN- 13: 978-9810863975.

OPEN ELEC TIV ES
Business Analytics

Teaching scheme Lecture: - 3 h/week

Course Code	**PGVES-302A**
Course Name	**Business Analytics**
Credits Prerequisites	–

Course objective

1. Understand the role of business analytics within anorganization.
2. Analyze data using statistical and data mining techniques and understand relationshipsbetween the underlying business processes of anorganization.
3. To gain an understanding of how managers use business analytics to formulate and solve business problems and to support managerial decisionmaking.
4. To become familiar with processes needed to develop, report, and analyze businessdata.
5. Use decision-making tools/Operations researchtechniques.
6. Mange business process using analytical and managementtools.
7. Analyze and solve problems from different industries such as manufacturing, service, retail,software, banking and finance, sports, pharmaceutical, aerospaceetc.

LECTURE WITH BREAKUP	NO. OF LECTURES
Unit I: Business analytics: Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of Business Analytics Process and organisation, competitive advantages of BusinessAnalytics. Statistical Tools: Statistical Notation, Descriptive Statistical metho d s, Review of probability distribution and data modelling, sampling and estimation methodsoverview.	9
Unit 2: Trendiness and Regression Analysis: Modelling Relationships and Trends in Data, simple LinearRegression. Important Resources, Business Analytics Personnel, Data and models for Business analytics, problem solving, Visualizing and Exploring Data, Business AnalyticsTechnology.	8
Unit 3: Organization Structures of Business analytics,Teammanagem e n t , Management Issues, Designing Information Policy, Outsour cing, Ensuring Data Quality, Measuring contribution of Business analytics, Managing Changes. Descriptive Analytics, predictive analytics, predicative Modellin g, Predictive analytics analysis, Data Mining, Data Mining Methodologi es, Prescriptive analytics and its step in the business analytics Process, Prescriptive Modelling, nonlinearOptimization.	9
Unit 4: Forecasting Techniques: Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonalit y, Regression Forecasting with Casual Variables, Selecting Appropriate ForecastingModels. Monte Carlo Simulation and Risk Analysis: Monte Carle Simulation Using Analytic Solver Platfom1, New-Product Development Model, Newsven dor Model, Overbooking Model, Cash BudgetModel.	10
Unit 5: Decision Analysis: Formulating Decision Problems, Decision Strategies with the without Outcome Probabilities, Decision Trees, The Value of lnformation, Utility and DecisionMaking.	8

Unit 6: Recent Trend s in : Embedded and collaborative business intelligence, Visual data recoverv, Data Storv telling and Data journalism.	4

COURSE OUTCOMES

1. Students will demonstrate knowledge of dataanalytics.
2. Students will demonstrate the ability of think critically in making decisions based on data and deepanalytics.
3. Students will demonstrate the ability to use technical skills in predicative and prescriptive modeling to support businessdecision-making.
4. Students will demonstrate the ability to translate data into clear, actionableinsights.

References :

1. Business analytics Principles, Concepts, and Applications by Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, Pearson FTPress.
2. Business Analytics by James Evans, personsEducation.

PGVES-302B: Open Electives: Industrial Safety [Sem – III]
3(L) (36 Lectures) CREDIT-3

Teaching Scheme Lectures: 3 hrs/week

Syllabus Contents:

Unit-I: Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure , describe salientpoints of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment andmethods.

Unit-II: Fundamentals of maintenance engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance , Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life ofequipment.

Unit-III: Wear and Corrosion and their prevention: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

Unit-IV: Fault tracing: Fault tracing-concept and importance, decision treeconcept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equ ipment's like, I. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler, vi. Electrical motors, Types of faults in machine tools and their generalcauses.

Unit-V: Periodic and preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhau ling of mechanical component s, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept andimportance.

References:

1. Maintenance Engineering Handbook, Higgins &Morrow, Da InformationServices.
2. Maintenance Engineering, H. P. Garg, S. Chand andCompany.
3. Pu mp-hydraulic Compressors, Audels, Mcgraw HillPublication.
4. Foundation Engineering Handbook, Winterkorn, Hans, Chapman & HallLondon.

PGVES-302C: Open Electives: Operations Research [Sem – III]
3(L) (36 Lectures) CREDIT-3

Teaching Scheme Lectures: 3 hrs/week

Course Outcomes:

At the end of the course, the student should be able to

1. Students should able to apply the dynamic programming to solve problems of discreet and continuousvariables.
2. Students should able to apply the concept of non-linearprogramming
3. Students should able to carry out sensitivityanalysis
4. Studentshouldabletomodeltherealworldproblemandsimulateit

Syllabus Contents:

Unit 1:
Optimization Techniques, Model Formulation, models, General LR Formulation, Simplex Techniques, Sensitivity Analysis, Inventory Control Models

Unit 2:
Formulation of a LPP - Graphical solution revised simplex method - duality theory - dual simplex method - sensitivity analysis - parametricprogramming

Unit 3:
Nonlinear programming problem - Kuhn-Tucker conditions min cost flow problem - max flow problem - CPM/PERT

Unit 4:
Scheduling and sequencing - single server and multiple server models - deterministic inventory models - Probabilistic inventory control models - Geometric Programming.

Unit 5:
Competitive Models, Single and Multi-channel Problems, Sequencing Models, Dynamic Programming, Flow in Networks, Elementary Graph Theory, Game Theory Simulation

References:

1. H.A. Taha, Operations Research, An Introduction, PHI,2008
2. H.M. Wagner, Principles of Operations Research, PHI, Delhi,1982.
3. J.C. Pant, Introduction to Optimization: Operations Research, Jain Brothers, Delhi,2008
4. Hitler Libermann Operations Research: McGraw Hill Pub.2009
5. Pannerselvarn, Operations Research: Prentice Hall of Ind ia2010
6. Harvey M Wagner, Principles of Operations Research: Prentice Hall of India2010

PGVES-302D: Open Electives: Cost Managem ent of Engineering Projects [Sem – III]
3(L) (36 Lectures)CREDIT-3

Teaching Scheme Lectures: 3 hrs/week

SyllabusContents:

Introduction and Overview of the Strategic Cost Management Process

Cost concepts in decision-making; Relevant cost, Differential cost, Incremental cost and Opportunity cost. Objectives of a Costing System; Inventory valuation; Creation of a Database for operational control; Provision of data forDecision-Making.

Project: meaning, Different types, why to manage, cost overruns centres, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and non• technical activities. Detailed Engineering activities. Pre project execution main clearances and documents Project team: Role of each member. Importance Project site: Data required with significance. Project contracts. Types and contents. Project execution Project cost control. Bar charts and Network diagram. Project commissioning: mechanical and process.

Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis. Various decision-making problems. Standard Costing and Variance Analysis. Pricing strategies: Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector. Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning, Total Quality Management and Theory of constraints. Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis. Budgetary Control; Flexible Budgets; Performance budgets; Zero-based bud gets. Measurement of Divisional profitability pricing decisions including transferpricing.

Quantitative techniques for cost management, Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Simulation, Learning CurveTheory.

References:

2. Cost Accounting A Managerial Emphasis, Prentice Hall of India, New Delhi
3. Charles T. Homgren and George Foster, Advanced Management Accounting
4. Robert S Kaplan Anthony A. Alkinson, Management &CostAccounting
5. Ashish K. Bhattacharya, Principles &Practices of Cost Accounting A. H. Wheeler publisher
6. N.D. Vohra , Quantitative Techniques in Management, Tata McGraw Hill Book Co.Ltd.

PGVES-302E: Open Electives: Composite Materials [Sem – III]
3(L) (36 Lectures) CREDIT-3

Teaching Scheme
Lectures: 3 hrs/week

SyllabusContents:

UNIT - I: INTRODUCTION: Definition - Classification and characteristics of Composite material s Advantages and application of composites. Functional requirements of reinforcement and matrix. Effect o reinforcement (size, shape, distribution, volume fraction) on overall compositeperformance.

UNIT – II: REINFORCEMENTS: Preparation- layup, curing, properties and applicatio n s of glass fibers, carbon fibers, Kevlar fibers and Boron fibers. Properties and applications of whiskers, particle reinforcements. Mechanical Behavior of composites: Rule of mixtures, Inverse rule of mixtures. Isostrain and Isostress conditions.

UNIT - III: Manufacturing of Metal Matrix Composites: Casting - Solid State diffusion technique, Cladding – Hot isostatic pressing. Properties and applications. Manufacturi n g of Ceramic Matrix Composites: Liquid Metal Infiltration - Liquid phase sintering. Manufacturing of Carbon - Carbon composites:Knitting, Braiding, Weaving. Properties and applications.

UNIT - IV: Manufacturing of Polymer Matrix Composites: Preparation of Moulding compoundsandprepregs–hand layupmethod–Autoclavemethod–Filamentwinding method – Compressionmoulding -Reaction injection moulding. Properties and applications.

UNIT – V: Strength: Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygrothermal failure. Laminate first play failure-insight strength; Laminate strength-ply discount truncated maximumstrain
criterion; strength design using caplet plots; stress concentrations.

TEXT BOOKS:

1. MaterialScienceand Technology–Vol13–Composites byR.W.Cahn–VCH,WestGermany.
2. Materials Science and Engineering, An introduction. WD Callister, Jr., Adaptedby R Balasubramanian1, John Wiley & Sons, NY, Indian edition, 2007.

References:

1. Hand Book of Composite Materials- ed-Lubin.
2. Composite Materials-K.K.Chawla.
3. Composite Materials Science and Applications -Deborah D.LChung.
4. Composite Materials Design and Applications – Danial Gay, Suong V. Hoa, and Stephen W.Tasi.

PGVES-302F: Open Electives: Waste to Energy [Sem – III]
3(L) (36 Lectures) CREDIT-3

Teaching Scheme
Lectures: 3 hrs/week

SyllabusContents:

Unit-I: Introduction to Energy from Waste: Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW - Conversion devices - Incinerator s, gasifiers, digestors

Unit-II: Biomass Pyrolysis: Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application - Manufacture of pyrolytic oils and gases, yields and applications.

Unit-III: Biomass Gasification: Gasifiers –Fixed bed system –Downdraft and updraft gasifiers – Flu idized bed gasifiers – Design, construction and operation – Gasifie r burner arrangem ent for thermal heating – Gasifier engine arrangem ent and electrical power – Equilibrium and kinetic consideration in gasifier operation.

Unit-IV: Biomass Combustion: Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustor s.

Unit-V: Biogas: Properties of biogas (Calorific value and composition) - Biogasplant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants -Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energyconversion
- Biomass energy programme in India.

References:

1. Non Conventional Energy, Desai, Ashok V., Wiley Eastern Ltd.,1990.
2. Biogas Technology - A Practical Hand Book - Khandel wal, K. C. and Mahdi, S. S., Vol. I &II, Tata McGraw Hill Publishing Co. Ltd.,1983.
3. Food, Feed and Fuel from Biomass, Challal, D. S., IBH Publishing Co. Pvt. Ltd.,199 1.
4. Biomass Conversion and Technology, C. Y. WereKo-Brobby and E. B. Hagan,John Wiley & Sons, 1996.

PGVES-381: M.Tech. Project Phase-I (Dissertation Phase-I) [Sem – III]
20(P) (240 Practical Hours) CREDIT-10

Teaching Scheme
Lab work : 20 hrs/week

Course Outcomes:

At the end of this course, students will be able to

- Ability to synthesize knowledge and skills previou sly gained and applied to an in- depth study and execution of new technicalproblem.
- Capable to select from different methodologies, methods and forms of analysis to produce a suitable research design, and justify theirdesign.
- Ability to present the findings of their technical solution in a writtenreport.
- Presenting the work in International/ National conference or reputedjournals.

Syllabus Contents:

The dissertation/project topic should be selected/chosen to ensure the satisfaction of the urgent need to establish a direct link between education, national development and productivity and thus reduce the gap between the world of work and the world of study. The dissertation should have thefollowing

- Relevance to social needs ofsociety
- Relevance to value addition to existing facilities in theinstitute
- Relevance to industryneed
- Problems of nationalimportance
- Research and development in various domain The student

should complete thefollowing:

- Literature survey ProblemDefinition
- Motivation for study andObjectives
- Preliminary design/feasibility/modularapproaches
- Implementation andVerification
- Report andpresentation

The dissertation stage I is based on a report prepared by the students on dissertation allotted to them. It may be basedon:

- Experimental verification *I* Proof ofconcept.
- Design, fabrication, testing of CommunicationSystem.
- The viva-voce examination will be based on the above report andwork.

Guidelines for Dissertation Phase- I M.Tech. Dissertation:

- As per the AICTE directives, the dissertation is a year long activity, to be carried out and evaluated in Phase -I: July to December.
- The dissertation may be carried out preferably in-house i.e. departments laboratories and centers OR in industry allotted through departments T & P coordinator.
- After multiple interactions with guide and based on comprehensive literature survey, the student shall identify the domain and define dissertation objectives. The referred literature should preferably include IEEE/IET/IETE/Springer/Science Direct/ACM journals in the areas of Computing and Processing (Hardware and Software), Circuits- Devices and Systems, Communication-Networking and Security, Robotics and Control Systems, Signal Processing and Analysis and any other related domain. In case of Industry sponsored projects, the relevant application notes, while papers, product catalogues should be referred and reported.
- Student is expected to detail out specifications, methodology, resources required, critical issues involved in design and implementation and phase wise work distribution, and submit the proposal within a month from the date of registration.
- Phase – I deliverables: A document report comprising of summary of literature survey, detailed objectives, project specifications, paper and/or computer aided design, proof of concept/functionality, part results, A record of continuous progress.
- Phase – I evaluation: A committee comprising of guides of respective specialization shall assess the progress/performance of the student based on report, presentation and Q & A. In case of unsatisfactory performance, committee may recommend repeating
  the Phase-I work.

SEMESTER IV

PGVES-481 : M.Tech. Project Phase-II (Dissertation Phase-II)
[Sem – IV] 32(P) (384 Practical Hours) CREDIT-16

Teaching Scheme
Lab work : 32 hrs/week

Course Outcomes:

At the end of this course, students will be able to

- Ability to synthesize knowledge and skills previously gained and applied to an in- depth study and execution of new technical problem.
- Capable to select from different methodologies, methods and forms of analysisto
  produce a suitable research design, and justify their design.
- Ability to present the findings of their technical solution in a written report.
- Presenting the work in International/ National conference or reputed journals.

Syllabus Contents:

The dissertation stage II is based on a report prepared by the students on dissertation allotted to them. It may be basedon:

- Experimental verification / Proof of concept.
- Design, fabrication, testing of Communication System.

The viva-voce examination will be based on the above report and work.

Guidelines for Dissertation Phase- IIM.Tech. Dissertation:

- As per the AICTE directives, the dissertation is a year long activity, to be ca rried out andevaluatedinPhase–II:JanuarytoJune.
- The dissertation may be carried out preferably in-house i.e. departments laboratories andcenters OR in indu stry a llotted through d epa rtments T & P coordinator.
- After multiple interactions with guide and based on comprehensive litera ture survey, the student sha ll identify the doma in and define dissert ation objectives. The referred litera ture should preferably include IEEE/IET/IETE/Springer/Science Direct/ACM journals inthe
  areas of Computing and Processing (Ha rdwa re and Software), Circuits-Devices and

Systems, Communication-Networking and Security, Robotics and Control Systems, Signal Processing and Analysis and any other related domain. In case of Indu stry sponsored projects, the relevant application notes, while papers, product catalogu es should be referred andreported.

- Student is expected to detail out specification s,methodology,resourcesrequired, critical issues involved in design and implementation and phase wise work distribution, and submit the proposal within a month from the date ofregistration.
- During phase – II, student is expected to exert on design, development and testing of the proposed work as per the schedule. Accomplished resu lts/contributions/innovat ion s should be published in terms of research papers in reputed journals and reviewed focused conferences ORIP/Patents.
- Phase – II deliverables: A dissertation report as per the specified format, developedsystem in the form of hardware and/or software, A record of continuousprogress.
- Phase – II evaluation: Guide along with appointed external examiner shall assessthe progress/performance of the student based on report, presentation and Q &A. Incase of unsatisfactory performance , committee may recommend for extensionor repeating the work

NB: This Syllabus is Board of Studies (BOS) approved.
BOS date: 12.11.2021.
Academic Council Date: 25.11.2021.