Maulana Abul Kalam Azad University of Technology, West Bengal

(Formerly West Bengal University of Technology)

Syllabus for M. Tech in Microelectronics and VLSI Technology(MVD)

(Applicable from the academic session 2023-2024)

MAULANA ABUL KALAM AZAD
UNIVERSITY OF TECHNOLOGY,
WEST BENGAL

THE DEPARTMENT OF
MICROELECTRONICS AND VLSI TECHNOLOGY

SYLLABUS

FOR POST GRADUATE DEGREE COURSE (M.Tech)

IN

Microelectronics and VLSI Technology

Maulana Abul Kalam Azad University of Technology, West Bengal

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VISION OF THE UNIVERSITY

To achieve the status of a globally ranked premier University in the field of Science, Technology, Pharmacy, Architecture, Management, and interdisciplinary areas for the creation of high-caliber professionals with environmental consciousness, social, moral, and ethical values along with the competency to face the new challenges of rapid technological advancements.

MISSION OF THE UNIVERSITY

To impart quality and value-based teaching & learning of international standards for solving the real-life problems

- To create and disseminate knowledge both nationally & internationally towards the transformations of the civilization into a knowledge-based society
- To institutionalize the extension and field outreach activities with a view to transforming the university system into an active instrument for social change
- To develop liaison and collaboration with globally recognized academic institutions in order to inject new and fresh thinking into teaching, learning, and research
- To generate intellectually capable and imaginatively gifted professionals and successful entrepreneurs having environmental consciousness and ethics who can work as an individual or in a group in multi-cultural global environments for continuing significantly towards the betterment of the quality of human life.

The vision of the Department of Microelectronics and VLSI Technology

The Department of Microelectronics and VLSI Technology envisions being a leader in pursuit of knowledge and wisdom for the holistic development of the rapid technological advancements of society in multi-disciplinary areas through excellence in teaching, training, and research and aspires to meet the global and socio-economic challenges of the state as well as a country.

Mission statements of the Department of Microelectronics and VLSI Technology (MS)

MS-1: To participate in the Special Man Power Development Program to meet the ever-challenging issues in the field of Microelectronics and VLSI Technology

MS-2: To enable the students to formulate, design, and solve problems in applied science and engineering.

MS-3: To provide excellent teaching and research environment using state-of-the-art facilities.

MS-4: To provide adequate support in developing knowledge-based skills to meet the requirements of the Microelectronics, Embedded Systems, & VLSI industry.

MS-5: To develop a positive attitude among students to participate in collaborative research work.

Program Educational Objectives (PEOs)

PEO-1: Students will be able to analyze, design, and implement VLSI Systems. They will learn to apply modern skills, techniques, and engineering tools to create VLSI Devices, Circuits and Systems.

PEO-2: Students will be able to understand the state of the art in the recent areas of research and develop a right attitude to perform original work collaboratively in order to contribute to the advancement of Microelectronics and VLSI Technology.

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PEO-3: Students will be able to participate in developing society, industry and economy.

PEO-4: Students will be able to achieve conceptual knowledge-based skill to meet the man-power demand of the upcoming semiconductor IC Design & Fabrication Industry.

Mapping Program Educational Objectives (PEOs) with Mission Statements (MS)

	MS-1	MS-2	MS-3	MS-4	MS-5
PEO-1	3	3	3	3	1
PEO-2	3	3	3	3	1
PEO-3	2	3	3	3	2
PEO-4	3	3	2	3	3

Note: '3' in the box for high-level mapping, 2 for Medium-level mapping, and 1 for 'Low-level' mapping.

Program Outcomes (POs)

After completion of this M.Tech program, the students will be able to –

PO-1. Independently carry out research /investigation and development work to solve practical problems.

PO-2. Write and present a substantial technical report/document.

PO-3. Demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor's program

PO-4. Employ professional and intellectual integrity and ethics of research for the requirement of sustainment in the advanced Academics or Industry.

Program Specific Outcomes (PSOs)

After completion of this M.Tech program, the students will be able to –

PSO-1: Achieve conceptual knowledge-based skill to meet the man-power demand of upcoming semiconductor IC Design & Fabrication Industry.

PSO-2: Apply the knowledge in analyzing the cutting-edge problems of Microelectronics, VLSI Device and Technology for their implementation in future integrated circuits.

PSO-3: Acquire professional and intellectual integrity and ethics of research for the requirement of sustaining in the advance Academics or Industry.

Mapping of Program Outcomes (POs) and Program Specific Outcomes (PSOs) with Program Educational Objectives (PEOs)

	PEO-1	PEO-2	PEO-3	PEO-4	PEO-5
PO-1	3	3	3	2	3
PO-2	1	3	2	2	3
PO-3	2	2	2	1	2

PO-4	3	3	2	3	3
PSO-1	3	3	2	3	3
PSO-2	2	3	3	3	2
PSO-3	2	2	2	2	3

Note: ‘3’ in the box for ‘high-level’mapping, 2 for ‘Medium-level’mapping, 1 for ‘Low-level’ mapping.

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Semester-wise Course Schedule

Semester – I

SL. NO.	CODE	PAPER NAME	L	T	P	MARKS	CREDIT POINTS
1.	**PGMVD-101**	Research Methodology	2	0	0	100	2
2.	**PGMVD-102**	Physics Of VLSI Devices	3	1	0	100	4
3.	**PGMVD-103**	Processor Architecture & SOC Design	2	0	0	100	2
4.	**PGMVD-104**	Microelectronics Technology	3	1	0	100	4
5.	PGMVD-105	Digital VLSI Circuits & Systems	3	0	0	100	3
6.	PGMVD-106	Audit Course – I	2	0	0	0	0
		Total Theory				**500**	**15**
7.	PGMVD-191	Microelectronics Lab-I	0	0	3	100	2
8.	PGMVD-192	VLSI Design - Lab-I	0	0	3	100	2
9.	PGMVD-193	Seminar – Review of current research Papers				100	2
		Total Practical and Sessional				**300**	**6**
		Total				800	21

Semester – II

SL. NO.	CODE	PAPER NAME	L	T	P	MARKS	CREDIT POINTS
1.	**PGMVD-201**	Analog VLSI Circuits & Systems	3	0	0	100	3
2.	**PGMVD-202**	**Testing & Verification of Digital Systems**	2	0	0	100	2
3.	**PGMVD-203**	A: Digital Signal Processing and Application B. Advanced communications System	3	0	0	100	3
4.	**PGMVD-204**	Advanced Micro & Nano Devices	3	0	0	100	3
5.	PGMVD-205	Advanced Engineering Mathematics	2	0	0	100	2

6.	PGMVD-206	Audit Course – II	2	0	0	0	0
		Total Theory				**500**	**13**
6.	PGMVD-291	Micro Electronics Lab-II	0	0	3	100	2
7.	PGMVD-292	VLSI Design Lab-II	0	0	3	100	2
8.	PGMVD-293	Term paper leading to Thesis			2	100	2
		Total Practical and Sessional				300	6
		Total				**800**	**19**

Semester – III

SL. NO.	CODE	PAPER NAME	L	T	P	MARKS	CREDIT POINTS
1.	**PGMVD-301**	A. Operating System B. Computer Organization C. Algorithms	3	0	0	100	3
		Total Theory				**100**	**3**
2.	PGMVD-391	Project Part-I	0	0	4	100	4
3.	PGMVD-392	Project Defense				100	4
4.	PGMVD-393	Group Project	0	0	3	100	3
		Total Sessional				300	11
		Total				**800**	**14**

Semester – IV

SL. NO.	CODE	PAPER NAME	L	T	P	MARKS	CREDIT POINTS
1.	**PGMVD-491**	Project Part –II	0	0	6	100	10
3.	**PGMVD-492**	Comprehensive Viva-voce				100	4
		Total				**200**	**14**

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Detailed Syllabus

SEMESTER – I

PGMVD-101: Research Methodology
[Sem – I] (L:2 T:0; P:0) (25 Lectures) CREDIT-2

Teaching Scheme
Lectures: l hrs/week

Course Outcomes:

At the end of this course, students will be able to

CO1: Identify the research problem.
CO2: Review research related information and Generalize research ethics
CO3: Debate on the control of today's world by Computer, Information Technology, whereas tomorrow world will be ruled by ideas, concept, and creativity.
CO4: Predict that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
CO5: Judge that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

Syllabus Contents:

Unit 1: Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem.

Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

Unit 2: Effective literature studies approaches, analysis Plagiarism, Research ethics,

Unit 3: Effective technical writing, how to write report, Paper; Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

Unit 4: Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

Unit 5: Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

Unit 6: New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

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References:

- Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students"'
- Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"
- Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners"
- Halbert, "Resisting Intellectual Property", Taylor &Francis Ltd,2007.
- Mayall, "Industrial Design", McGraw Hill,1992.
- Niebel, "Product Design", McGraw Hill,1974.
- Asimov, "Introduction to Design", Prentice Hall,1962.
- Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New Technological Age", 2016.
- T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand,2008

CO-PO Mapping

CO	PO1	PO2	PO3	PO4
CO1	2	2	3	3
CO2	2	2	3	2
CO3	2	2	3	3
CO4	2	2	3	2
CO5	2	1	3	3

Note: '3' in the box for high-level mapping, 2 for Medium-level mapping, and 1 for 'Low-level' mapping.

Department: Microelectronics and VLSI Technology **Year:**1st **Course Name:** Physics of VLSI Devices **Credit:** 4	**Session:**2023-2024 **Semester:** I **Course Code:** PGMVD102 **Target Student:** PG **Contact:** (L:3; T:1; P:0)

Pre-requisite: Knowledge of basic physics of Semiconductors, Junctions and Devices – diodes, BJTs, FETs, MOS structures.

Module – 1: Introduction to VLSI Design

What is an integrated circuit, IC? History of IC development, Different types of IC, Introduction to VLSI, Moore's Law & VLSI Devices.

Module – 2: Recapitulation and Orientation

P-n junction diode: Background study of Physics of Junctions, Device structure, Depletion region, Static

behaviour, Dynamic or Transient behaviour, Drift-diffusion model, Diode model and model parameters.

Module – 3: MOS as a Two-terminal Device
Two-terminal MOS structure: MOS Device at equilibrium, Flat Band Condition, Effect of Gate Voltage & Surface Potential: Accumulation, Depletion and Inversion, Flat-Band Voltage, Threshold Voltage, MOS as a Capacitor: Ideal Capacitance-Voltage Characteristics, Frequency Effects, Effect of Oxide Charge & Interface Charge on Flat-Band Voltage & Threshold Voltage, C–V Measurement as a Diagnostic tool in MOS Device Process Control MOS Capacitor Model.

Module – 4: MOSFET as Three & Four-terminal VLSI Device
Three & Four-terminal MOSFET Device Structure, Enhancement type MOSFET, Depletion Type MOSFET, Circuit Symbols, MOSFET Current-Voltage Characteristics & Regions of Operation: Concepts, Long-Channel MOSFET: Gradual Channel Approximation, Pao-Sah Model Equation for MOSFET, Pinch-off Effect, Channel-Length Modulation, Early effect, Body effect, Subthreshold Characteristics, MOSFET channel mobility, Punch through. Impact of aspect ratio in MOSFET performance
MOSFET Performance parameters: Threshold Voltage, I ON /I OFF, On-resistance, Sub-threshold Swing, Transconductance, Output Conductance.

Module – 5: MOSFET Device Models
Threshold Voltage Modeling, Derivation of Pao-Sah Model Equation, Transconductance Modeling, Mobility Model,
MOSVAR Model, SPICE Equivalent Model: Large Signal Model, Small Signal Model: Miller Capacitance, Effect of Miller Capacitance on MOSFET performance, Gain & Cut-off Frequency of a MOSFET. Study of Nanostructure: Use of Density-function Theory (DFT).

Module – 6: CMOS as VLSI Device:
Basic CMOS Device: Static and Dynamic Characteristics, Parameter Extraction

Text Book:
1. Ben G. Streetman, Sanjay Kumar Banerjee, Solid State Electronic Devices, Pearson,
Donald A. Neamen, Semiconductor Physics and Devices, Basic Principles, McGraw Hill
2. Yuan Taur & Tak H. Ning, Fundamental of Modern VLSI Devices, Cambridge University Press
Reference Book:
1. Yannis Tsividis, Operation and modelling of the MOS Transistor (second edition) (Oxford)
2. Philip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design (second edition) (Oxford)
3. Simon Sze, Ming-Kwei Lee, “Semiconductor Devices, Physics and Technology”, Third Edition, Wiley
Additional Learning Materials:
1. Presentation prepared by the teacher
2. NPTEL lectures.

Course Outcomes:
- Apply the knowledge of basic semiconductor material physics and analyze the characteristics of various electronic devices
- To make the student conversant with the VLSI chip; In this context the importance of the Physics of the devices that make up the chip are to be highlighted.
- The fundamental Physics of the Devices, with special emphasis on the MOSFET should be explained.

- The effects of scaling of device dimensions for inclusion in the VLSI chip are to be enumerated and analyzed.
- Finally, the methods used to overcome the limitations in the context of the devices as they appear in the VLSI chip are to be included.

CO-PO Mapping

Subject	Course Outcomes	POs			
		1	**2**	**3**	**4**
Physics of VLSI Devices	1. Apply the knowledge of basic semiconductor material physics and analyze the characteristics of various electronic devices	2	1	2	3
	2. To make the student conversant with the VLSI chip; In this context the importance of the Physics of the devices that make up the chip are to be highlighted.	3	1	2	2
	3. The fundamental Physics of the Devices, with special emphasis on the MOSFET should be explained.	1	1	1	3
	4. The effects of scaling of device dimensions for inclusion in the VLSI chip are to be enumerated and analyzed.	2	1	2	2
	5. Finally, the methods used to overcome the limitations in the context of the devices as they appear in the VLSI chip are to be included.	2	1	2	2
Note: '3' in the box for '**high-level'mapping**, 2 for '**Medium-level'mapping**, 1 for '**Low-level' mapping**.					

Department: Microelectronics and VLSI Technology **Year:** 1st **Course Name:** Processor Architecture & SOC Design **Contact:** (L: 2; T: 0; P: 0)	**Session:**2023-2024 **Semester:** I **Course Code:** PGMVD103 **Target Student:** PG **Credit:** 2

Prerequisite:
Digital Electronics and logic design with a thorough knowledge about state machine design**.** Familiarization with algorithm and programming concept, FPGA boards may be used for the laboratory, along with design/simulation tools as and when necessary.

Course Objectives:
i) Student should learn the basic and advanced concepts of processor & memory architecture and designing

processor and memories. They should also know the performance matrix and how to enhance performance of the processor
ii) Student should learn High Performance Computing
iii) Student should learn SoC Design
.

1**. Processor Architecture: (4L)**
a) Concept of Computer Systems, Basic building blocks, Store and forward concept, Von-Neumann Architecture, Introduction to Processor and Processor Organization. (2L)
b) Processor Architecture: Instruction Set Architecture: Instructions & Addressing, Procedures and Data, Instruction Set Variations. (2L)
2. Datapath Design: (4L)
a) The Arithmetic/ Logic Unit: Number Representation, Adders and Simple ALUs, Multipliers and Dividers, Floating-Point Architecture. Carry Look Ahead adders, Carry Save adder, Pipelined array multiplier, Pipelined adder (4L)
3. Control unit design: **(6L)**
a) Hardwired control unit, Micro-program-controlled unit, Nano Program Control Unit (4L)
b) RISC and CISC Architectures. Harvard architecture, VLIW architecture. (2L)
4. Memory Design: (3L)
a) Concept of Volatile and non-volatile memory, ROM, EPROM, EEPROM, Static RAM, Dynamic RAM, Cache memory, Primary and secondary cache, cache cohesion (3L)
5. Performance Enhancement of Processor by Pipelining: (6L)
a) Basic idea to enhance the performance of a processor, Concept of Pipelining, Pipeline performance, various hazards in the pipeline, and methods to solve the hazards. (2L)
b) Pipeline performance measurement parameters- speedup, efficiency, throughput, classification of pipeline processor, pipeline structure of CPU, examples from the design of arithmetic pipeline- floating point adder, Multifunction pipeline, reservation table, Dynamic pipeline. (2L)
c)Vector Processing: a) Characteristics of vector processing, vector instructions, differences between scalar and vector processing with example, Pipeline chaining. (2L)

6. High Performance Computing:(6L)
a) Performance measurement parameters – MIPS, MFLOPS, SPEC rating, CPI etc., introduction to high-performance computing – Overview, Flynn's classification – SISD, SIMD, MISD, MIMD (2L)
b) SIMD Array processors: SIMD computer organization, Masking and Data-Routing Mechanisms, Inter PE Communication, SIMD Inter Connection Networks, Loosely Coupled and Tightly Coupled Multiprocessors, MIMD computer organization(4L)

7. Introduction to SOC and FPGA Architecture and Design: (6L)
a) Concept of SOC, pSOC, SOC vs. processor on chip, FPGA concept, architecture and design flow.
b) SOC design issues: SOC architecture, SOC Design Flow, and Silicon power management, thermal management for low-power SOC design.
c) Reconfigurable architecture.

Books:
1. Computer Architecture & Organization J.P Hayes (McGraw Hill)
2. Hwang & Briggs, *Computer Architecture & Parallel Processing* (TMH)
3. Tien-Fu Chen, *Overview of SOC architecture design*, (National Chung Cheng University)

Reference Books:

1. Hwang, *Advanced Computer Architecture*, (TMH)

2. Patterson & Hennessy, *Computer Organization & Design,* (Morgan Kaufmann)
3. Stalling, *Computer organization and architecture, designing for performance*, (PHI)
4. Antonakos, *An Introduction to intel family of Microprocessors*, (Pearson)
5.. Flynn*, Computer Architecture*, (Narosa)
6. Tammy Noergaard*, Embedded Systems Architecture – a comprehensive guide for engineers and programmer*s, (Elsevier)
7. David A. Patterson and John L. Hennessy, Computer Organization and Design
8. Carl Hamachar, Zvonco Vranesic and Safwat Zaky, *The Hardware/Software Interface*, Elsevier.
9. William Stallings, *Computer Architecture and Organization*, McGraw Hill.
10. Vincent P. Heuring and Harry F. Jordan, *Computer Organization and Architecture: Designing*
11. A.Sinha, Processor Architecture (Lecture notes), MAKAUT

COURSE OUTCOME (CO)

1. To learn the Concept of a Computer System and Design methodology of Processor Design
2. To learn Datapath Design (Adder, Subtractor, multiplier etc.)
3. To learn the design of hardwired control unit, microprogrammed and nano programmed Control unit.
4. To learn Memory Technology & design various types of memory units and memory Organization.
5. To learn the concept of Performance Enhancement of Processor by Pipelining, SOC architecture, FPGA architecture, design, and Reconfigurable Architecture

CO-PO Mapping

Subject	Course Outcomes	Program Outcomes			
		1	2	3	4
Processor Architecture and System On Chip design	**1. To learn the Concept of a Computer System and Design methodology of Processor Design**	1	2	3	1
	2. To learn Datapath Design (Adder, Subtractor, multiplier etc.)	2	3	3	3
	3. To learn the design of hardwired control unit, microprogrammed and nano programmed Control unit.	2	3	3	3

	4. To learn Memory Technology & design various types of memory units and memory organization.	3	3	3	3
	5. To learn the concept of Performance Enhancement of Processor by Pipelining, SOC architecture, FPGA architecture, design and Reconfigurable Architecture	3	3	3	3
Note: '3' in the box for '**high-level'mapping**, 2 for '**Medium-level'mapping**, 1 for '**Low-level' mapping**.					

Department: Microelectronics and VLSI Technology **Year:** 1st **Course Name:** Microelectronics Technology **Credit:** 4	**Session:**2023-2024 **Semester:** I **Course Code:** PGMVD104 **Target Student:** PG **Contact:** (L: 3; T: 1; P: 0)

Module-1: Introduction to Microelectronics Technology
Historical Perspective of Development of IC, Introduction to Integrated Circuits, Silicon as a Material of choice for VLSI Chip, Semiconductor Manufacturing; Fundamentals of Device Fabrication Processes & their Significance. Isolation Technique: LOCOS / STI. 2L

Module – 2: Silicon Wafer Engineering – Ingot to Industry Ready Wafer
Si Ingots and Wafer, Si Crystal Growth: Electronic Grade Silicon, Czochralski Growth, Wafer Characterization and Wafer Specifications/Properties. 4L

Module- 3: Concept of Clean Room & Wafer Cleaning and Etching 8L
Wafer cleaning as a unit Process, Surface Contaminants: Organic, Inorganic & Metal, Cleaning Methods: Solvent Method, Pirhanah Cleaning & RCA Cleaning of Si Wafer, Concept of Clean Room.
Laboratory Practices under PGMVD-191: Cleaning of p-type & n-type Si-Wafer by Solvent Method, Piranha Cleaning RCA cleaning
Etching – Introduction to Etch Process, Issues in Etching, Types of Etching: Wet & Dry Etching, Basic Mechanism of Etching, Etch parameters,
Isotropic and Anisotropic Etching, Selectivity, Isotropy and Etch Bias, Bias and Degree of Anisotropy; Common Wet Etchants, Orientation Dependent Etching Effects; Plasma Etch Mechanisms, Reactive Ion Etching, Selective Etchant.
Laboratory Practices under PGMVD-191: Simulation of Si Wafer Etching using TCAD Silvaco/Synopsys Athena, Finding the Etch Process Parameters, Laboratory Standard Isotropic & Anisotropic Etching

Module 4: Process Oxidation 8L
Introduction to Thermal Oxidation Process, Properties, Function of Oxide Layer, Growth Mechanism and Kinetics of Oxidation, Deal-Grove Model, Oxidation Rate Constants, Types of Oxidation: Dry and Wet Oxidant, Properties of Silicon-di-Oxide, Oxide Induced Defects,
Characterization of Oxide Films; Dopant Redistribution, Oxide Charges, Quality of Oxide Layer, Device Isolation: Local Oxidation (LOCOS)
Laboratory Practices under PGMVD-191: Simulation of Oxidation of Si or Growth of SiO 2 by using TCAD Silvaco/Synopsys and Characterization & Process Parameter Extraction.

Module 5: Diffusion & Ion Implementation
Introduction to Diffusion Process in Si Wafer & its Modelling: Fick's Law, Pre-Deposition and Drive-in Diffusion Modeling, Characterization of Impurity Profiles & Process Parameters.
Laboratory Practices under PGMVD-191: Simulation of Diffusion of Dopants in Si Wafer using TCAD Silvaco/Synopsys 4L

Module 6: Ion implantation
Problems in Thermal Diffusion & Ion Implantation, Process & Its Modeling, Range theory, Depth Profile, Ion Implant Distributions Profile,
Process Parameters, Ion Implantation Damage, Post Implantation Annealing: Rapid Thermal Annealing, Ion Channeling, High energy and Multi Energy Implantation.
Laboratory Practices under PGMVD-191: Simulation of Doping through Ion Implantation in Si Wafer using TCAD Silvaco/Synopsys Athena 6L

Module 7: Lithography
Overview of Lithography, Components of Photolithography- Masks, Photolithography & Pattern Transfer: Operational Principle, Types of Photolithography: Contact/Proximity and Projection Printing, Resolution, Depth of Focus, Resist Processing Methods and Resolution Enhancement. Introduction to ITRS Road map. Introduction to next-generation Lithography: Resolution of the photo-lithographic system and Critical Dimension. 6L

Module 8: Metallization
Overview, Contact Metallization, Different types of metallization techniques: Physical Vapor Deposition: Thermal evaporation, Electron Beam Evaporation, Problems in Aluminum Metal contacts, Al and Junction spiking, Electro Migration
Laboratory Practices under PGMVD-191: Simulation of Metallization or Deposition of Aluminium contact on Si wafer using TCAD Silvaco/Synopsys Athena. 4L

Module 9: Process Integration & CMOS Technology
Integration of processes for CMOS Technology: N well, P-well, NMOS and Twin tub CMOS and its uses & challenges, Packaging, System on Chip

Text Book:

• Simon Sze, Ming-Kwei Lee, "Semiconductor Devices, Physics and Technology", Third Edition, Wiley
• Campbell, The Science and Engineering of Microelectronic Fabrication, Oxford University Press
• S. K. Gandhi, VLSI Fabrication Principles: Silicon and Gallium Arsenide, John Wiley & Sons, Inc.

Reference Book:

• Morgan, D.V., and Board, K , An Introduction to Semiconductor Microtechnology
• The National Technology Roadmap for Semiconductors , Notes: Semiconductors Industry Association, SIA, 1994
• Sze, S.M. , Electrical and Electronic Engineering Series VLSI Technology, Mcgraw-Hill International Editions

Course Outcomes: Students must be able to

- appreciate the role of material Silicon in VLSI chips.
- have a clear concept of the Unit Processes and their specific application area.
- understand the fabrication of a complete device.
- assess the different performance parameters of the unit process of a VLSI chip and comment on how to optimize the performance.

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- Understand the steps involved in nano device processing applied in Semiconductor manufacturing industry.

CO-PO Mapping

Subject	Course Outcomes	POs			
		1	**2**	**3**	**4**
Microelectronics Technology	1. Appreciate the role of material Silicon in VLSI chips.	**2**	1	**2**	3
	2. Have a clear concept of the Unit Processes and their specific application area.	**2**	1	2	2
	3. Understand the fabrication of a complete device.	**1**	1	**1**	**3**
	4. Assess the different performance parameters of the unit process of a VLSI chip and comment on how to optimize the performance.	**2**	**2**	**2**	2
	5. Understand the steps involved in nano device processing applied in Semiconductor manufacturing industry.	2	1	2	2
Note: '3' in the box for '**high-level'mapping**, 2 for '**Medium-level'mapping**, 1 for '**Low-level' mapping**.					

Department: Microelectronics and VLSI Technology **Year:** 1st **Course Name: Digital VLSI Circuits & Systems** **Contact:** (L: 3; T: 0; P: 0)	**Session:**2023-2024 **Semester:** I **Course Code:** PGMVD105 **Target Student:** PG **Credit:** 3

Prerequisite: Basic concept of Digital Logic - combinatorial & sequential logic design, Digital Laboratory, Basic concept of BJT and MOS transistors.

Principal Objective:

- To make the student conversant with the VLSI chip design
- Special emphasis on the MOSFET should be explained.
- The effects of scaling of device dimensions for inclusion in the VLSI chip are to be enumerated and analyzed.
- Finally the methods used to overcome the limitations in the context of the devices as they appear in the VLSI chip are to be included.

1: Introduction to VLSI Design (4 Lectures)

Basics of Integrated Circuit (IC), SSI, MSI, LSI, VLSI, ULSI, Integration levels. History of IC

development, Moore's Law, Different types of IC chips; Digital, Analog & Mixed signal ICs; Different Domains of VLSI design; EDA- the VLSI design CAD tools, VLSI design state-of-the-art, some emerging applications of VLSI, VLSI design complex processor, VLSI Design Flow, Synthesis, layout generation, Verification and simulation, VLSI chip manufacturing process flow, Overview on latest industry development on VLSI design, Introduction to disaggregated architecture.

2: **CMOS logic Basics (6 Lectures)**
Basics of MOS transistors and MOS as switches, Complementary CMOS logic, CMOS logic behaviour, advantages and drawbacks of CMOS logic, Pull-up and pull-down network, conduction complement, complex logic function using CMOS, pass transistors, transmission gates, tri-state buffers, Flip- flops (D-F/F, JK F/F etc.), transistor count, Delay, drawbacks of CMOS, Dynamic logic, Domino logic, Bi-CMOS to overcome the drawbacks of CMOS, standard cell design, full custom design. example of a standard cell., Sequential Logic circuits –asynchronous and synchronous sequential circuits, Moore machine, Mealy machine, examples, Finite state machine design.

3. Basics of CMOS fabrication and Layout: (6)
Introduction to VLSI fabrication and fabrication steps, Concept of MASK, Lithography, etching, polysilicon patterning, ion implementation, metallization etc., fabrication error, concept of layout, feature size, Lambda rule, concept of process technology, stick diagram, general design rules for layout, width spacing rule, poly diffusion interaction, contacts, VIA and contact spacing, examples of CMOS layout of an inverter, NAND/NOR gates, simplified design rule, full custom and standard cell layout, placement, routing, floor planning. Interconnect, Different Problems of interconnect: Crosstalk, Ohmic Drop, Electromigration and their solutions.

4. Hardware description language & EDA tools (6)
EDA tools and their advantages, concept of test bench, simulation, design verification, synthesis, hardware description language (HDL)-VHDL/VERILOG/SYSTEM C etc.

5. Programmable Hardware and FPGA (6)
Concept of Programmable Hardware (PLA, PLD, CPLD, FPGA) and their requirements, FPGA --Architecture, configuration and design flow, system design using FPGA, concept of System on Chip (SOC). FPGA as reconfigurable computing and programmable System on Chip (pSOC). FPGA as validation of custom design or ASIC.

6. Logical Effort (4)
Logical effort-Path Logical Effort, Path Electrical Effort, Path Effort, branching effort, delay in a logic gate, path effort delay, path parasitic delay, designing fast circuits and gate sizes, multistage logic networks, choosing the best number of stages, delay **vs.** fan out.

7. Design of a 32-bit RISC CPU and 1K-8 bit RAM (6)
Designing a RISC CPU with fixed instruction length (32-bit) CPU , few instructions , Static RAM design with 1024 locations with each word size of 8 bits, Simulation, Synthesis & validation of the architecture on FPGA and analysis of the performance of the CPU with a small program written in machine language.

Text:
1. Introduction to VLSI Systems—Carver Mead, Lynn Conway, B.S. Publication

2. Chip Design for Submicron VLSI-- John P Uyemura, Thompson Publication.

1. Advanced CMOS cell Design: Etienne Scard., Sonia Delmas Bendhia, McGraw Hill Professional.
2. VLSI Design Black Book—K.V.K.K. Prasad, Kattula Shyamala, dreamtech Publication
3. A Verilog HDL Premier, 2nd edition, J. Bhaskar, BS Publication

References:

1. Fundamentals of Modern VLSI Devices by Yuan Taur & Tak H. Ning (Cambridge)
2. Logic and Computer Design Fundamentals—M. Morris Mano and Charles R.Kime, Pearson Education.
3. Digital Design | With an Introduction to the Verilog HDL, VHDL, and, System Verilog| by M. Morris Mano and Michael D. Ciletti Sixth Edition, Pearson
4. CMOS Analog Circuit Design (second edition) Phillip E. Allen and Douglas R. Holberg (Oxford).
5. The MOS Transistor (second edition) Yannis Tsividis (Oxford)
6. NPTEL lectures & certification modules.
7. Russell, G, Kinniment, D.J., Chester, E.G., and McLauchlan, M.R., *CAD for VLSI* Notes: Van Norstrand Rheinhold, 1985.
8. Neil Weste and David Harris, *CMOS VLSI Design: A Circuits and Systems Perspective* (3rd Edition).

COURSE OUTCOME(CO)

1.To learn the basics of Integrated Circuit (IC): different Domains of VLSI design, design automation tools and the state-of-the-art VLSI circuits.
2. To learn CMOS logic behaviour, advantages and drawbacks using static, dynamic, Domino-logic and Bi-CMOS logic, logical effort, path effort, path effort delay, path parasitic delay, designing fast circuits and multistage logic networks and the concept of delay **vs.** fan out
3. To learn the basics of CMOS fabrication and Layout.
4. To learn EDA tools and their advantages, concept of test bench, simulation, design verification, synthesis and hardware description language (Verilog)
5. To learn the concept of Programmable Hardware and their requirements, FPGA --architecture, configuration and design flow, concept of System on Chip (SOC) and FPGA as validation of custom design or ASIC, the design of a 32-bit RISC CPU, Static RAM and Simulation, Synthesis & validation of the architectures on FPGA and analysis their performances.

CO -PO Mapping

Subject	Course Outcomes	Program Outcomes

Maulana Abul Kalam Azad University of Technology, West Bengal

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		1	2	3	4
Digital VLSI Circuits & Systems	1. To learn the basics of Integrated Circuit (IC); different Domains of VLSI design, design automation tools and the state-of-the-art VLSI circuits.	2	2	1	1
	2. To learn CMOS logic behaviour, advantages and drawbacks using static, dynamic, Domino-logic and Bi-CMOS logic, logical effort, path effort, path effort delay, path parasitic delay, designing fast circuits and multistage logic networks and the concept of delay **vs.** fan out	2	2	1	1
	3. To learn the basics of CMOS fabrication and Layout.	2	2	1	1
	4. To learn EDA tools and their advantages, concept of test bench, simulation , design verification , synthesis and hardware description language(Verilog)	2	2	1	1
	5. To learn the concept of Programmable Hardware and their requirements, FPGA --architecture, configuration and design flow, concept of System on Chip (SOC) and FPGA as validation of custom design or ASIC, the design of a 32-bit RISC CPU, Static RAM and Simulation, Synthesis & validation of the architectures on FPGA and analysis their performances.	2	3	3	3
Note: '3' in the box for '**high-level'mapping**, 2 for '**Medium-level'mapping**, 1 for '**Low-level' mapping**.					

PGMVD106 : Audit I : English for Research Paper Writing
[Sem – I] (L:2; T:0; P:0) (25 Lectures) CREDIT-0

Course objectives:

Students will be able to:

- Understand that how to improve your writing skills and level of readability
- Learn about what to write in each section
- Understand the skills needed when writing a Title Ensure the good quality of paper at very first-time submission

Syllabus

Units	CONTENTS	Hours
1	Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity	4

2	Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism,	4
3	Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.	4
4	key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the	4
5	skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions	4
6	useful phrases, how to ensure paper is as good as it could possibly be the first- time submission	4

SuggestedStudies:

1. Goldbort R (2006) Witting for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highm a n 'sbook.
4. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London , 2011

PGMVD106 : Audit I : Disaster Management
[Sem – I] (L:2; T:0; P:0) (25 Lectures)
CREDIT-0

Course Objectives:

Students will be able to:

1. learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
2. critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
3. develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
4. critically understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countries they work in

Syllabus

Units	CONTEN TS	Hours
1	**Introduction** Disaster: Definition, Factors And Significance; Difference Between Hazard And Disaster; Natural And Manmade Disasters: Difference, Nature, Types And Magnitude.	4

2	**Repercussions Of Disasters And Hazards**: Economic Damage, Loss Of Human And Animal Life, Destruct ion Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.	4
3	**Disaster Prone Areas in India** Study Of Seismic Zones; Areas Prone To Floods And Droughts, Landslides And Avalanches; Areas Prone To Cyclonic And Coastal Hazards With Special Reference To Tsunami ; Post-Disaster Diseases And Epidemics	4
4	**Disaster Preparedness And Management** Preparedness: Monitoring Of Phenomena Triggering A Disaster Or Hazard; Evaluation Of Risk: Application Of Remote Sensing, Data From Meteorological And Other Agencies, Media Reports: Governmental And Community Preparedness.	4
5	**Risk Assessment** Disaster Risk: Concept And Elements, Disaster Risk Reduction, Global And National Disaster Risk Situation. Techniques Of Risk Assessment, Global Co-Operation In Risk Assessment And Warning, People's Participation In Risk Assessment. Strategies for Survival.	4
6	**Disaster Mitigation** Meaning, Concept And Strategies Of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation And Non-Structural Mitigation, Programs Of Disaster Mitigation In India.	4

SUGGESTED READINGS:

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'NewRoyal bookCompany.
2. Sahni, Pardeep Et.AL (Eds.)," Disaster Mitigation Experience s And Reflections", Prentice Hall Of India, NewDelhi.
3. Goel S. L. , Disaster Administration And Management Text And Case Studies" ,Deep &DeepPublication Pvt. Ltd., NewDelhi.

PGMVD106 : Audit I : Sanskrit for Technical Knowledge [Sem – I] (L:2; T:0; P:0) (25 Lectures) CREDIT-0

Course Objectives

1. To get a working knowledge in illustrious Sanskrit, the scientific language in the world
2. Learning of Sanskrit to improve brain functioning

3. Learning of Sanskrit to develop the logic in mathematics, science &other subjects enhancing the memory power
4. The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from ancient literature

Syllabus

Unit	Content	Hours
1	• Alphabets in Sanskrit, • Past/Present/Future Tense, • Simple Sentences	8
2	• Order • Introduction of roots • Technical information about Sanskrit Literature	8
3	• Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics	8

Suggested reading

1. "Abhyaspustakam"- Dr. Vishwas , Samskrita-Bh arti Publication,New Delhi
2. "Teach Yourself Sanskrit" Prathama Deeksha-Vempati Kutumbshastri, Rashtriya SanskritSansthanarn, New DelhiPublication
3. "India 's Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., NewDelhi.

Course Output

Students will be able to

1. Understanding basic Sanskritlanguage
2. Ancient Sanskrit literature about science & technology can beunderstood
3. Being a logical language will help to develop logic instudents

PGMVD106 : Audit I : Value Education [Sem – I] (L:2; T:0; P:0) (25 Lectures) CREDIT-0

Course Objectives

Students will be able to

1. Understand value of education and self-development
2. Imbibe good values in students
3. Let the should know about the importance of character

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Syllabus

Unit	Content	Hours
1	• Values and self-development -Social values and individual attitudes. Work ethics, Indian vision of humanism. • Moral and non- moral valuation. Standards and principles. • Value judgments	4
2	• Importance of cultivation of values. • Sense of duty, Devotion, Self-reliance. Confidence, Concentration . Truthfulness, Cleanliness. • Honesty, Humanity. Power of faith, National Unity. • Patriotism. Love for nature, Discipline	6
3	• Personality and Behavior Development - Soul andScientific attitude. Positive Thinking. Integrity and d iscipline. • Punctuality, Love andKindness. • Avoid faultThinking. • Free from anger, Dignity oflabour. • Universal brotherhood and religioustolerance. • Truefriendship. • Happiness vs suffering, love fortruth. • Aware of self-destructivehabits. • Association and Cooperation. • Doing best for savingnature	6
4	• Character and Competence -Holy books vs Blind faith. • Self-management and Good health. • Science of reincarnation. • Equality, Nonviolence ,Humility, Role of Women. • All religions and same message. • Mind your Mind, Self-control. • Honesty, Studying effectively	6

Suggested reading

1. Chakroborty, S.K. "Values and Ethics for organizations Theory and practice", Oxford University Press, New Delhi

Course outcomes

Students will be able to

1. Knowledge of self-development
2. Leam the importance of Human values
3. Developing the overall personality

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PGMVD106 : Audit I : Constitution of India [Sem – I] (L:2; T:0; P:0) (25 Lectures) CREDIT-0

Course Objectives:

Students will be able to:

1. Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
2. To address the growth of Indian opm10n regarding modern Indian intellectuals ' constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
3. To address the role of socialism In India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.

Syllabus

Units	Content	Hour
1	• **History of Making of the Indian Constitution:** History Drafting Committee, (Composition & Working)	4
2	• **Philosophy of the Indian Constitution:** Preamble Salient Features	4
3	• **Contours of Constitutional Rights & Duties:** • Fundamental Rights • Right to Equality • Right to Freedom • Right against Exploitation • Right to Freedom of Religion • Cultural and Educational Rights • Right to Constitutional Remedies • Directive Principles of State Policy • Fundamental Duties.	4
4	• **Organs of Governance:** • Parliament • Composition • Qualifications and Disqualifications • Powers and Functions • Executive • President • Governor • Council ofMinisters • Judiciary, Appointm ent and Transfer of Judges,Qualifications • Powers andFunctions	4

5	• **LocalAdministration:** • District'sAdministrationhead:RoleandImportance, • Municipalities:Introduction, Mayor and role of Elected Representative, CEC of MunicipalCorporation. • Pachayatiraj:Introduction,PRI:ZilaPachayat. • Electedofficialsandtheirroles,CEOZilaPachayat:Positionandrole. • Blocklevel:OrganizationalHierarchy(Differentdepartments), • Villagelevel:RoleofElectedandAppointedofficials, • Importance of grass rootdemocracy	4
6	• **ElectionCommission:** • ElectionCommission:RoleandFunctioning. • Chief Election Commissioner and Election Commissioners. • StateElectionCommission:RoleandFunctioning. • InstituteandBodiesforthewelfareofSC/ST/OBCandwomen.	4

Suggested reading

1. TheConstitutionofIndia,1950(BareAct),GovernmentPublication.
2. Dr.S.N.Busi,Dr.B.R.AmbedkarframingofIndianConstitution,lstEdition,2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn.,Lexis Nexis, 2014.
4. D.D.Basu, IntroductiontotheConstitutionofIndia,LexisNexis,2015.

CourseOutcomes:

Students will be able to:

l.Discuss thegrowthof thedemandforcivilrightsinIndiafor thebulkofIndiansbefore thearrivalofGandhiinIndianpolitics.

2. Discuss the intellectualorigins of the framework of argument that informed theconceptualization of social reforms leading to revolution inIndia.
3. Discuss the circumstancessurrounding the foundation of the Congress Socialist Party[CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposalof direct elections through adult suffrage in the IndianConstitution.
4. Discuss the passage of the Hindu Code Bill of1956.

PGMVD106 : Audit I : Pedagogy Studies [Sem – I] (L:2; T:0; P:0) (25 Lectures) CREDIT-0

Course Objectives:

Students will be able to:

4. Review existing evidence on the review topic to inform programme designand policy making undertaken by the DfID, other agencies andresearchers.
5. Identify critical evidence gaps to guide thedevelopment.

Syllabus

Units	Content	Hours

1	• Introduction andMethodology: • Aims and rationale, Policy background, Conceptual framework andterminology • Theories of learning, Curriculum , Teachereducation. • Conceptual framework, Researchquestions. • Overview of methodology andSearching.	4
2	• Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developingcountries. • Curriculum,Teachereducation.	2
3	• Evidence on the effectiveness of pedagogicalpractices • Methodology for the in depth stage: quality a ssessment of included studies. • How can teacher education (curriculu m and practicum) and the school curricu lum and guidance materials best support effectivepedagogy? • Theory ofchange. • Strength and nature of the body of evidence for effectivepedagogicalpractices. • Pedagogic theory and pedagogicalapproaches. • Teachers'attitudesandbeliefsandPedagogicstrategies.	4
4	• Professional development: alignment with classroom practicesand follow-up support • Peersupport • Support from the head teacher and thecommunity. • Curriculum andassessment • Barriers to learning: limited resources and large cla sssizes	4
5	• Researchgapsandfuturedirections • Researchdesign • Contexts • Pedagogy • Teacher education • Curriculum andassessment • Dissemination and resea rchimpact.	2

Suggested reading

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2):245-261.
2. Agrawal M (2004) curricular reform in schools: The importance of evaluation, Journal of Curriculum Stud ies, *36* (3):361-379.
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi- site teacher education research project (MUSTER) country report 1. London: D FID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (20 13) Improving teaching and learning of Basic math and reading in Africa: Does teacher preparation count? International Journal Educational Development, *33* (3):272-282.
5. Alexander RJ (200 1) Culture and pedagogy: International comparisons in primary education.Oxford and Boston:Blach-well.
6. Chavan M (2003) Read India: A mass scale, rapid, 1earning to read'campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf

Course Outcomes:

Students will be able to understand:

1. What pedagogical practices are being used by teachers in formal and informal classrooms in developingcountries?
2. What is the evidence on the effectiveness of these pedagogical practices, in what conditions, andwith what population oflearners?
3. How can teacher education (curriculum and practicum) and the school curriculum and guidancematerials best support effectivepedagogy?

PGMVD106 : Audit I : Stress Management by Yoga [Sem – I]
(L:2; T:0; P:0) (25 Lectures) CREDIT-0

Course Objectives

1. To achieve overall health of body andmind
2. To overcom estress

Syllabus

Unit	Content	Hours
1	• Definitions of Eight parts of yog. (Ashtanga)	8
2	• Yam and Niyam.Do's and Don't's inlife. i) Ahinsa, satva, astheva, Bramhacharva andaparigraha ii) Shaucha, santosh, tapa, swadhyav,Ishwarpranidhan	8
3	• Asan andPranayam i) Various yog poses and their benefits for mind &body ii) Regularization of breathing techniques and its effects-Types of pranayam	8

Suggested reading

1. 'Yogic Asanas for Group Tarining-Part- 1" : Janardan Swami Yogabhyasi Mandal,Nagpur
2. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda , Advaita Ashrama (Publication Department) ,Kolkata

Course Outcomes

Students will be able to:

1. Develop healthy mind in a healthy body thus improving social health also
2. Improve efficiency

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PGMVD106 : Audit I : Personality Development through Life Enlightenment Skills [Sem – I] (L:2; T:0; P:0) (25 Lectures) CREDIT-0

Course Objectives

1. To learn to achieve the highest goalhappily
2. To become a person with stable mind, pleasing personality anddetermination
3. To awaken wisdom in student s

Syllabus

Unit	Content	Hours
1	Neetisatakam-Holistic development of personality • Verses- 19,20,2 1,22(wisdom) • Verses- 29,31,32 (pride &heroism) • Verses- 26,28,63,65(virtue) • Verses- 52,53,59 (dont's) • Verses- 71,73,75,78(do's)	8
2	• Approach to day to day work andduties. • Shrimad Bhagwad Geeta : Chapter 2-Verses 41,47,48, • Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23,35, • Chapter 18-Verses 45, 46,48.	8
3	• Statements of basicknowledge. • Shrimad Bhagwad Geeta: Chapter 2 - Verses 56, 62,68 • Chapter 12 - Verses 13, 14, 15, 16,17,18 • Personality of Role model. Shrimad Bhagwad Geeta:Chapter 2 - Verses 17, Chapter 3 - Verses36,37,42, • Chapter 4 - Verses 18,38,39 • Chapter 1 8 - Verses37,38,63	8

Suggested reading

1. "Srimad Bhagavad Gita" by Swami Swarupananda Advaita Ashram (Publication Department), Kolkata
2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P. Gopinath, Rashtriya Sanskrit Sansthanam, NewDelhi.

CourseOutcomes

Students will be able to

1. Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal inlife
2. The person who has studied Geeta will lead the nation and mankind to peace andprosperity
3. Study of Neetishatakam will help in developing versatile personality ofstudents.

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Department: Microelectronics and VLSI Technology **Year:** 1st **Course Name: Microelectronics Lab-I** **Credit:** 2	**Session:**2023-2024 **Semester:** I **Course Code:** PGMVD191 **Target Student:** PG **Contact:** (L: 0; T: 0; P: 3)

1. Cleaning the substrate by using Solvent Method.
   - Glass Substrate
   - Silicon substrate (P-type and n-type)

2. Cleaning the n-type and p-type water for further processing / Thin film deposition using following methods:-
   - Solvent method.
   - Piranha Method.
   - RCA Cleaning method.

3. Etching of a cleaned P-type Si-wafer by using HF:HNO3 in required Stoichiometric volume.
   - Study the sample under compound microscope and Study illumination of the sample under UV light.

4. Study the etching rate under environmental condition:-
   - Isotropic etching.
   - Anisotropic etching.

5. Contact metallization on Si wafer by using Physical Vapour Deposition (PVD Technique)
   - Ohmic contact.
   - Schottky contact.

6. Contact metallization on Si wafer by using Electron Beam Evaporation ()
   - Ohmic contact.
   - Schottky contact.

7. Contact Metallization by depositing Thin Film Coating
   - By using Spin Coating method.

COURSE OUTCOME(CO)

After completion of this course students are able

1. To get familiar about Cleaning the substrate by using Solvent Method
2. To get familiar about Etching of a cleaned P-type Si-wafer
3. To Study the etching rate under environmental condition
4. To Understand about the Contact metallization on Si wafer

CO -PO Mapping

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Subject	Course Outcomes	Program Outcomes			
		1	2	3	4
Microelectronics Lab-I	1. To get familiar about Cleaning the substrate by using Solvent Method	3	3	2	1
	2. To get familiar about Etching of a cleaned P-type Si-wafer	3	3	3	2
	3. To Study the etching rate under environmental condition	2	2	3	2
	4. To Understand about the Contact metallization on Si wafer	3	2	3	3
Note: '3' in the box for '**high-level'mapping**, 2 for '**Medium-level'mapping**, 1 for '**Low-level' mapping**.					

Department: Microelectronics and VLSI Technology **Year:** 1st **Course Name: VLSI Design - Lab-I** **Credit:** 2	**Session:**2023-2024 **Semester:** I **Course Code:** PGMVD192 **Target Student:** PG **Contact:** (L: 0; T: 0; P: 3)

Course Objective:

1- student will be familiar about the steps involved in VLSI design.
2- students will be able to write program in hardware definition language (HDL) like Verilog.
3- student will be able to design the digital circuit on VLSI design Tools like Xilinx ISE / Icarus Verilog.
4- students will be able to write the Test Bench program for simulation.
5- student will be able to Validate the design of circuit by Test Bench in iSim/GTK Wave Simulator.
6- student will be able to make Bit-stream file and download into FPGA.

Pre-requisite: Knowledge of programming, Basic gates, Digital Circuits – Combinational & Sequential

Part-A: FPGA Based Digital Design

Software & Hardware Tools – Xilinx ISE, VIVADO, FPGA Boards

LAB – 1A: Introduction to FPGA Based Digital Design:

- Register-transfer-level abstraction
- Introduction to HDL Coding by Basic Digital Gates
- Using Xilinx ISE Pack for HDL Coding, Simulation & Synthesis

LAB – 1B: Understanding the FPGA Board

- Identifying the Board Parts
- Procedure of Bit-Stream Downloading by Basic Digital Gates
- JTAG

LAB – 2: Writing Verilog Code, Test Bench for Simulation & Synthesis

- Combinational Circuit – Multiplexer, Demultiplexer, Decoder, Encoder, Half Adder, Full Adder, Half Subtractor, Full Subtractor, Adder- Subtractor.

LAB – 3: Writing Verilog Code, Test Bench for Simulation & Synthesis

- Combinational Circuit – Ripple Carry, Carry look ahead adder
- Construction of Higher Level Multiplexer using Lower Level Multiplexer
- Circuit Designing using universal logic: Multiplexer

LAB – 4: Writing Verilog Code, Test Bench for Simulation & Synthesis
- Sequential Circuit –
- Flip-Flop – SR, D, JK, T

LAB – 5: Writing Verilog Code, Test Bench for Simulation & Synthesis
- Sequential Circuit –
- Counter – Up, Down, Bidirectional, Ring, Ripple, Johnson, Mod-N.

LAB – 6: Writing Verilog Code, Test Bench for Simulation & Synthesis
1. Sequential Circuit –
2. Register – Left/Right Shift Register, Construction of Memory.

LAB – 7: Writing Verilog Code, Test Bench for Simulation & Synthesis
1. Sequential Circuit –
2. FSM – Mealy & Moore

LAB – 8: Writing Verilog Code, Test Bench for Simulation & Synthesis
1. ALU Design

Part-B: Front End Using Synopsys

Software – Synopsys, Centos/Linux

LAB – 9: Synopsys Front End - Introduction
- Using Verilog Compiler Simulator (VCS)
- Using DVE for analyze, compile and simulate
- Using Design Vision for Synthesis & Gate Level Net list preparation

LAB – 10: Synopsys Front End-Experiment
- Experiment with Up-Down Counter with above 3 modules
- Functionality Check
- Timing Analysis
- Power Analysis

Books:
1. Advanced Digital Design using Verilog-HDL, Michael. D. Ciletti, PHI publications.

COURSE OUTCOME(CO)

After completion of this course students are able

1. To get familiar about VLSI Design Tools like Xilinx, Icarus Verilog, GTK Wave
2. To Understand the difference between sequential language and concurrent language.
3. To Know about the Hardware Description Language (Verilog/VHDL) to describe the Combinatorial and Sequential logic as well as Test Bench for simulation.
4. To Understand about the FPGA Board and JTAG Cable and generate bit stream file and download to the programmable hardware device: FPGA.
5. To get familiar about front-end design tool: Synopsys and understand the hardware realization of the design by Synthesis Steps: High level Synthesis, logic Synthesis, physical Synthesis.

CO -PO Mapping

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Syllabus for M. Tech in Microelectronics and VLSI Technology(MVD)

(Applicable from the academic session 2023-2024)

Subject	Course Outcomes	Program Outcomes			
		1	2	3	4
VLSI Design Lab-I	CO1. Familiar about VLSI Design Tools like Xilinx, Icarus Verilog, GTK Wave.	1	2	3	2
	CO2. Understand the difference between sequential language and concurrent language.	1	3	2	2
	CO3. Know about the Hardware Description Language (Verilog/VHDL) to describe the Combinatorial and Sequential logic as well as Test Bench for simulation.	1	2	2	2
	CO4. Understand about the FPGA Board and JTAG Cable and generate bit stream file and download to the programmable hardware device: FPGA.	1	2	2	2
	CO5. To get familiar about front-end design tool: Synopsys and understand the hardware realization of the design by Synthesis Steps: High level Synthesis, logic Synthesis, physical Synthesis.	1	2	2	3
Note: '3' in the box for '**high-level'mapping**, 2 for '**Medium-level'mapping**, 1 for '**Low-level' mapping**.					

SEMESTER – II

Department: Microelectronics and VLSI Technology **Year:**1st **Course Name:** Analog VLSI Circuits & Systems **Contact:** (L: 3; T: 0; P: 0)	**Session:**2023-2024 **Semester:** II **Course Code:** PGMVD201 **Target Student:** PG **Credit:** 3

Objectives:

1. To Design the single stage amplifiers using PMOS and NMOS driver circuits with different loads.
2. To Analyze high frequency concepts of single stage amplifiers and noise characteristics associated with differential amplifiers.
3. To Study the different types of current mirrors and to know the concepts of voltage and current reference circuits.
4. To Understand about MOS switched capacitor filters.
5. Apply the methods learned in the class to design and implement practical projects.

Sl. No	Module Name and Topics	Class hours
1	**Introduction:** Motivation for analog VLSI and mixed signal circuits in CMOS	2

	technologies and issues thereof.	
2	**CMOS device fundamentals:** Basic MOS models, device capacitances, parasitic resistances, substrate models, transconductance, output resistance, f_T, frequency dependence of device parameters.	6
3	**Single stage amplifiers, Differential Amplifiers:** Common source amplifier, source degeneration, source follower, common gate amplifier, cascade stage. Basic differential pair, common mode response, differential pair with MOS loads, Gilbert Cell, device mismatch effects, input offset voltage.	10
4	**Current Mirrors, Current and Voltage Reference:** Basic current mirrors, cascode current mirrors, active current mirrors, low current biasing, supply insensitive biasing, temperature insensitive biasing, impact of device mismatch.	4
5	**Frequency Response of Amplifiers, Feedback:** Miller effect, CS amplifier, source follower, CG amplifier, cascade stage, differential amplifier, Multistage amplifier. Feedback topologies, effect of load, modeling input and output ports in feedback circuits.	4
6	**Operational Amplifiers:** Performance parameters, One-stage and two-stage Op Amps, gain boosting, comparison, common mode feedback, input range, slew rate, power supply rejection, noise in Op Amps.	8
7	**Other Sub-circuits**, **Field Programmable Analog array (FPAA):** Comparators; AD & DA conversion; Swiched-mode circuits – principle of operation.Concept of switch capacitor, Configurable analog block (CAB), Basic concept of FPAA, Architecture of FPAA, EDA tools, Application of FPAA.	6
	Total	40

Text:

1 CMOS Analog Circuit Design (second edition) Phillip E. Allen and Douglas R. Holberg (Oxford)

Reference:

1. Weste N and Eshraghian K; Addision Wesley 1985 ,*Principles of CMOS VLSI Design*
2. Mukherjee A , 1986, *Introduction to NMOS and CMOS VlSI Systems Design* , Prentice-Hall
3. Mead and Conway, *Introduction to VLSI System*s , Notes: Addison Wesley D C & Co

COURSE OUTCOME(CO)

After completion of this course students are able

1. Learn circuit design technique and design issues in CMOS technologies.

2. Gain knowledge of basic MOS models, device capacitances, parasitic resistances, transconductance, up to frequency dependence of device parameters.
3. Understand the significance of different biasing styles and apply them for different circuits.
4. Design basic building blocks like sources, sinks, mirrors, up to layout level and acquire computer skills (e.g. LT-spice) for the design and analysis of circuits.
5. Comprehend the design and analysis of MOS Op-Amp circuits and systems, identifying suitable topologies of the constituent sub systems and corresponding circuits as per the specifications of the system.

CO -PO Mapping

CO	PO1	PO2	PO3	PO4
CO1	2	2	3	3
CO2	2	2	3	3
CO3	2	2	3	3
CO4	2	2	3	3
CO5	2	2	3	3
Average	2	2	3	3

Note: '3' in the box for '**high-level'mapping**, 2 for '**Medium-level'mapping**, 1 for '**Low-level' mapping**.

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(Applicable from the academic session 2023-2024)

Department: Microelectronics and VLSI Technology **Year:** 1st **Course Name: Testing & Verification of Digital Systems** **Contact:** (L: 2; T: 0; P: 0)	**Session:** 2023-2024 **Semester:** II **Course Code:** PGMVD202 **Target Student:** PG **Credit:** 2

Module 1 (2 Hrs.) **(Introduction to VLSI Design Flow, concept of Testing & Verification)**	Introduction to VLSI Design (Flow, Synthesis, layout generation, Verification and simulation), background of testing of electronic circuits, basic concept of Testing & Verification and their differences, Automatic Testing equipment.
Module 2 (6 Hrs.) **(Testing in different stages of manufacturing, Design verification, and system level operation and testing)**	Testing in different stages of manufacturing, Design verification, chip yield, system-level operation and testing, different testing algorithms, EDA tools for testing
Module 3 (6 Hrs.) **(Test Pattern Generation and Fault Modelling)**	Concept of Automatic Test pattern Generation (ATPG), Fault coverage, Fault models, Stuck-at-1, stuck-at-0 faults, transistor faults, collapsed faults, bridging faults, Delay Faults and Crosstalk, pattern sensitivity and coupling faults.
Module 4 (6 Hrs.) **(Automatic Test Pattern Generation, different types of faults and Design for Testability)**	Automatic Test Pattern Generation (ATPG): Algorithms for generating a sequence of test vectors for a given circuit based on specific fault models. Fault analysis and Simulation to emulate fault models in CUT and application of test vectors to determine fault coverage: Parallel, deductive, and concurrent fault simulation, Design for testability, Scan, Built-in-self-test, Pseudo-random number generator, Automatic Test Generation, Built-in Logic Block observer (BILBO)
Module 5 (6 Hrs.) **(Boundary Scan and JTAG)**	Boundary Scan , JTAG (IEEE standard 1149.1) concept , Architecture and Instruction set and Boundary Scan TAP control operation .testing process using JTAG Testing of Analog and Mixed-signal circuits, Differences from digital testing , Test procedures, DSP based mixed signal test, Test plan , Boundary Scan Architecture & instruction Set of Mixed Signal Testing

	(IEEE1149.4) and test Process
Module 6 (6 Hrs.) **(Testing of Analog & mixed signal circuits)**	Different packages, Concept of Analog circuit testing, traditional concept of analog circuit testing and their limitations, specification-based test, different methods of functional testing, testing of Analog VLSI circuits, testing of mixed signal circuits, DSP based mixed signal circuit testing, waveform synthesizer/digitizer.
Module 7 (4 Hrs.) **(Boundary scan method for Testing of Analog & mixed signal circuits)**	boundary scan technique (IEEE 1149.4) method of using them for testing analog and mixed signal circuits IEEE 1149.4 Standard Analog Test Bus (ATB), Basic Mixed Signal Chip structure IEEE 1149. Digital /Analog Interfaces, Analog test access Port, Test Bus Interface circuit (TBIC), TBIC Switching Patterns, Chaining of 1149.4 compliance ICs.

Text Books:
1. Testing of Digital Systems" by N. K. Jha et.al.
2. Essentials of Electronic **Testing**" by M L Bushnell and V D Agrawal.
3. Digital Systems **Testing** and Testable **Design**" by M Abramovici and A D Friedman.

Reference Books:
1. Testing & Verification of VLSI circuits – Lecture notes by A.Sinha
2. Built-in **Test** for **VLSI**: Pseudorandom Techniques" by P H Bardell and J Savir

COURSE OUTCOME(CO)

After completion of this course students are able

1.To learn the step by step design flow of VLSI circuits and systems in details , the need of design verification & testing and the difference between testing and verification
2. To learn testing in different stages of manufacturing, Design verification, chip yield, system level operation and testing
3. To learn the concept of test vectors, test generation, different types of faults, fault modelling and to analyse the behaviour of the circuit under test (CUT)
4.To learn different algorithms of Automatic Test generation (ATPG) on specific fault models and fault simulation, Design for Testability (DFT) and different approaches and also

various techniques and methodologies used for testing different analog and mixed signal circuits.
5. To learn the concept of boundary scan technique and standardized test interface (IEEE standard 1149.1) to build capability of observing and controlling pins into each chip to make board test easier

CO -PO Mapping

Subject	Course Outcomes	Program Outcomes			
		1	2	3	4
Testing & Verification of VLSI circuits	1.To learn the step by step design flow of VLSI circuits and systems in details , the need of design verification & testing and the difference between testing and verification	2	2	3	3
	2.. To learn testing in different stages of manufacturing , Design verification ,chip yield, system level operation and testing	3	3	3	3
	3. To learn the concept of test vectors , test generation , different types of faults ,fault modelling and to analyse the behaviour of the circuit under test (CUT)	2	3	3	3
	4. To learn different algorithms of Automatic Test generation (ATPG) on specific fault models and fault simulation, Design for Testability (DFT) and different approaches and also various techniques and methodologies used for testing different analog and mixed signal circuits.	2	3	2	3
	5. To learn the concept of boundary scan technique and standardized test interface (IEEE standard 1149.1) to build capability of observing and controlling pins into each chip to make board test easier	2	3	3	3
Note: '3' in the box for '**high-level'mapping**, 2 for '**Medium-level'mapping**, 1 for '**Low-level' mapping**.					

Department: Microelectronics and VLSI Technology **Year:**1st **Course Name: Digital Signal Processing and Applications** **Contact:** (L: 3; T: 0; P: 0)	**Session:**2023-2024 **Semester:** II **Course Code:** PGMVD203 **Target Student:** PG **Credit:** 3

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Pre-requisites: 1] Signals and Systems ii] Advanced Engg. Maths iii]Digital Electronics iv] Computer Architecture & Organization / Processor Architecture

Course Objective:

This course is to make students familiar with the most important methods in DSP, including digital filter design, transform-domain processing , multi resolution signal Processing and importance of signal processors by providing a thorough knowledge of design , implementation and analysis of DSP systems .

Module 1: Introduction to Discrete-Time Signal & Systems (3L)

Concept of continuous time signal and discrete time signals, Discrete Analog and Digital signals & Systems. Advantages of Digital signal Processing Systems Analog Signal Processing Systems. Converting continuous signal to digital signal (Sampling, Quantization and coding): Study of sampling theorem, effect of under sampling.

i] Aliasing Problem: To analyze the effect of under-sampling a signal using MATLAB

ii] Study of Quantization of continuous-amplitude, discrete-time analog signals Quantization error

iii] Coding of quantized signal, different types of coding

Concept of ADC, DAC and Different types of ADC (Successive approximation, dual slope, pipelined, Flash, Sigma delta etc.) and DAC

2. Concept of continuous-time Fourier transform , discrete- time Fourier transform (DTFT), Discrete-Fourier Transform (DFT)and Fast Fourier Transform (FFT).

Continuous time Fourier Transform (3L)

Concept of continuous time Fourier transform and to derive equation for discrete time Fourier transform (DTFT) and analyze them using MATLAB, Computer discrete time Fourier transform of various signals, Properties of Discrete Time Fourier Transform, Discrete Fourier transform, decimation in time and decimation in frequency, Various properties of discrete time Fourier transform and verify these properties on various signals on MATLAB. Algorithm of Discrete Fourier Transform on MATLAB and to find discrete Fourier transform of various signals on MATLAB. Properties of discrete Fourier transform.

Module 2: Fast Fourier Transform (FFT) (3L)

Fast Fourier transform (FFT) algorithm and complexity analysis. To analyze fast Fourier algorithms and analyze using MATLAB. The architecture of DFT and FFT Processor.

Module 3: Z Transform (6)

Z – Transform: Basic concept, Transformation from S to Z Transformation, DTFT to Z Transformation, two-sided and one-sided Z Transform, Concept of unit circle and ROC, Stability, casualty, Properties of ROC, properties of Z Transform, Z Transformations of basic functions like unit impulse, step, exponential, Sine etc., Examples, inverse z transform, partial fraction method etc. Bi-linear transformation (relation between S and Z transformation), System Transfer Function, to understand basic building blocks like adder, multiplier and delay units of discrete-time systems, Transfer functions of Recursive and Non-Recursive filters and their different realization (Direct, Transpose, Cascade, Parallel etc.) of FIR and IIR Filters.

Module 4: Digital Filter Design (4L)

a) **FIR filter design** (Low pass, High Pass, Band Pass, Band stop) Linear phase FIR filter, Filter design using Fourier Transform, Gibbs Phenomenon, Goertzel Algorithm.

b) **IIR Filter design**, analog filter approximation and design of Butterworth, Chebychev and Elliptic filters.

c) **simulation** of Infinite Impulse Response (IIR) Filters and Finite Impulse Response (FIR) filters and analyzes their responses on MATLAB.

d) **Multi-Rate Signal Processing (2)**
Introduction, Why multi-rate Signal processing? Up Sampling , Down Sampling, rational sampling, CIC (Cascaded Integrated comb filtering)

e) **Adaptive Signal Processing (2)**

Introduction, LMS algorithm, Adaptive filtering with DCT/ LMS, Applications: Adaptive echo cancellation, Adaptive echo cancellation, fatal electrocardiography etc.

Module 5: Time-frequency analysis and introduction to wavelet transform. (4L)
Introduction**,** Time-frequency analysis**,** Limitation of Fourier transform**,** Short-term Fourier transform**,** Mathematical expression of Wavelet transforms and analysis**,** Wavelength transform algorithm and architecture. Application of wavelet transform

Module 6: DSP Architecture: (4)
Key features of DSP processors (MAC unit, circular addressing scheme, zero overhead looping , bit reversal technique , Pipelining , Harvard Architecture), Different DSP Processors and their Architectures, Implementation of DSP algorithms on 16 bit , 32 bit DSP Processors like TMS320 C30 , TMS 320 C65XX series DSP Processors , FPGA architecture, (, Xilinx Spartan 6E, Virtex 6, Artix 7 etc.) , Programming using HD and system design. Mapping DSP algorithms onto DSP Processors/ FPGA.

Module 7: DSP Applications (4L)
i] DTMF detection ii] LMS algorithm iii] Adaptive echo cancellation iv] Software Defined Radio/Cognitive Radio. Introduction to VLSI Signal Processing.

Text Books:
1. Digital Signal Processing -j.g. Proakis 7 D.G. Manolakis (Pearson Education)
2. Digital Signal Processing – S.K. Mitra (Tata Mcgraw- Hill Publishing Co.)
3. Digital Signal Processing -Andreas Antonio (Tata Mcgraw Hill Publishing Co.)

Reference Books:
1.Theory and Problems of Digital Signal Processing- M.H. Hayes (Tata Mcgraw- Hill Publishing Co.)
2. Digital Signal Processing- Steve White (Cengage Learning,India edition)
3. Digital Signal Processing & Applications with the TMS320C6713 and TMS320C6416 DSK – R. Chassing, Donald Reay (Willey student edition)
4. Digital Signal Processing – Lecture notes by A.Sinha 5.
Network analysis -Van Valkenburg (Prentice-hall of India Pvt. Ltd.)

COURSE OUTCOME(CO)

After completion of this course students are able

1.To learn the concept of Discrete Signals/Digital signals & Systems and their advantages over Analog Signal Processing systems
2. To learn Continuous Time Fourier Transform (CTFT), Discrete Time Fourier Transform (DTFT), Discrete Fourier Transform (DFT) , Fast Fourier Transform (FFT),
3.To learn the requisite mathematics (Z Transform) to model system behavior and their response to a given stimuli.
4.To learn and acquire design skills on frequency domain analysis of different filters such as FIR & IIR, multi-resolution filter and adaptive Filter using MATLAB, realization of Digital Filters on different hardware platforms (DSP Processors, FPGAs, advanced Signal Processors, FPGAs and ASICs.)
5. To learn in details about time frequency analysis and Wavelet transform, different applications of Digital Signal Processing like DTMF, Echo cancellation, SDR etc.

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CO -PO Mapping

Subject	Course Outcomes	Program Outcomes			
		1	2	3	4
Digital Signal Processing & Applications	1. To learn the concept of Discrete Signals/Digital signals & Systems and their advantages over Analog Signal Processing systems	2	2	2	1
	2.. To learn Continuous Time Fourier Transform (CTFT), Discrete Time Fourier Transform (DTFT), Discrete Fourier Transform (DFT) , Fast Fourier Transform (FFT),	3	3	3	3
	3. To learn the requisite mathematics (Z Transform) to model system behaviour and their response to a given stimuli	3	3	3	3
	4.To learn and acquire design skills on frequency domain analysis of different filters such as FIR & IIR, multi-resolution filter and adaptive Filter using MATLAB, realization of Digital Filters on different hardware platforms (DSP Processors, FPGAs, advanced Signal Processors, FPGAs and ASICs.)	3	3	3	3
	5. To learn in details about time frequency analysis and Wavelet transform, different applications of Digital Signal Processing like DTMF, Echo cancellation, SDR etc.	3	3	3	3
Note: '3' in the box for '**high-level'mapping**, 2 for '**Medium-level'mapping**, 1 for '**Low-level' mapping**.					

Department: Microelectronics and VLSI Technology **Year:** 1st **Course Name:** Advanced Micro and Nano Devices **Contact:** (L: 3; T: 0; P: 0)	**Session:**2023-2024 **Semester:** II **Course Code:** PGMVD204 **Target Student:** PG **Credit:** 3

Prerequisite:

Fundamentals of basics of p-n junctions, MOS capacitors, MOSFETs,

[Recapitulation of MOS Capacitor, CMOS, low and high frequency equivalent circuits of MOSFETs, MOSFET models]

Course content:

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Module-1 (14 lectures) – MOSFET Scaling and Small Geometry Effects

Different strategies of MOSFET scaling: Constant-Field Scaling, Constant-Voltage Scaling, Effect of scaling upon key Device Parameters

Short Channel & Narrow width Effect: Drain Induced Barrier Lowering, Channel Length Modulation, Mobility Degradation, Velocity Saturation Effects, Hot Electron Effects, Gate Induced Drain Leakage, Oxide Breakdown, Avalanche Breakdown, Snapback Breakdown, Threshold Voltage Roll-off, Gate Induced Drain Leakage, Reliability Issues in MOSFET.

Module-2 MOSFET Structural Engineering

Gate, Electrode & Contact Engineering: Metal Gate High-K Dielectric

Channel Engineering by using Doping Engineering & Material Engineering, Enhance Channel Mobility Materials and Strained Silicon FETs

Electrodes and Contact Engineering: Overview, Ohmic Contact, AI / Poly Silicon / Metal Gate, Schottky Contacts, Dual Metal Gate, Electrolyte Gate.

Module-3 (8 lectures) – Bandgap Engineering and Epitaxy

Band Gap Engineering: Compound Semiconductor, Silicon-Germanium Heterostuctures, Epitaxy and Vertical Scaling,

Concept of Critical Layer Thickness, Misfit Factor, Super lattice, Dislocation in Epitaxial Growth, Growth of Epitaxial layer: Homo and Hetero Epitaxy, Chemical Vapor Deposition (CVD)/Vapor Phase Epitaxy(VPE), Metalorganic Vapour-Phase Epitaxy (MOVPE), Molecular-Beam Epitaxy (MBE), Atomic Layer Deposition (ALD)

Advance Micro & Nano Devices: Advanced MOS Devices, Fully Depleted Silicon On Insulator (FD-SOI), Partially Depleted Silicon On Insulator (PDSOI), FinFETs, Junctionless MOSFET, Heterojunction, Device Based Quantum Wells: Concept and Introduction of to Modulation-Doped Field Effect Transistor (MODFET), High Electron Mobility Transistor (HEMT), Resonant Tunneling Diodes (RTD)

Module-4 (6 lectures) - Optical Properties of Semiconductor and Emerging Optoelectronic Devices, Photoconductivity,

Optical absorption, generation & transportation in Semiconductor, Photoluminescence, Fluorescence, Phosphorescence,

Solar Cell & Photo-detector: Basic operation, Principal, Device Performance, Parameter Extraction & Equivalent Model

Text Books:

1. Sung-Mo Kang, Yusuf Leblebici, “CMSO Digital Integrated Circuits, Analysis and Design.”, Tata McGraw Hill
2. Mark Lundstrom, Jing Guo, “Nanoscale Transistors, Device Physics, Modeling and Simulation”, Springer
3. Jan M. Rabay, Anantha Chandrakasan, Borivoje Nikolic, “Digital Integrated Circuits, A Design Perspecive” Second
Edition, Pearson
4. Simon Sze, Ming-Kwei Lee, “Semiconductor Devices, Physics and Technology”, Third Edition, Wiley
5. P. K. Bhattacharya, “Semiconductor Optoelectronic Devices”, Prentice Hall

Course outcomes: At the end of the course, students will be able to:

- CO1- Define the fabrication process steps for the design of nanometric CMOS devices.
- CO2- Employ the physical principles of spintronic devices, carbon nanotubes, graphene and optoelectronic devices.

- CO3- Compare the characteristics of different advanced electronic devices like HEMT, single electron transistors and resonant tunneling devices

- CO4- Systematize a fabrication procedure for a nanometric CMOS IC with the proper technological process for the materials of the substrate, implanted areas, isolation, metallisation.

- CO5- Analyze a solar cell from its extracted electrical parameters.

CO-PO Mapping

Subject	Course Outcomes	POs			
		1	2	3	4
Advanced Micro and Nano Devices	1. Define the fabrication process steps for the design of nanometric CMOS devices.	2	1	2	3
	2. Employ the physical principles of spintronic devices, carbon nanotubes, graphene and optoelectronic devices.	2	1	2	2
	3. Compare the characteristics of different advanced electronic devices like HEMT, single electron transistors and resonant tunneling devices	1	1	1	**3**
	4. Systematize a fabrication procedure for a nanometric CMOS IC with the proper technological process for the materials of the substrate, implanted areas, isolation, metallisation.	2	2	2	1
	5. Analyze a solar cell from its extracted electrical parameters.	2	2	2	2
Note: '3' in the box for '**high-level'mapping**, 2 for '**Medium-level'mapping**, 1 for '**Low-level' mapping**.					

Department: Microelectronics and VLSI Technology **Year:**1st **Course Name:** Advanced Engineering Mathematics	**Session:**2023-2024 **Semester:** I **Course Code:** PGMVD205 **Target Student:** PG **Contact: L:2; T:0; P:0 (Credit Point:2)**

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(Applicable from the academic session 2023-2024)

Module-I:
Fourier series and Transform: Revision of Fourier series, integrals and transforms and their properties. The 2-dimensional fourier transform, convolution theorem, Parseval's formula, discrete fourier transform, fast fourier transform .

Module-II:
Z-transforms: sequence, representation of sequence, basic operations on Sequences, z-transforms, properties of z transforms, change on scale, shifting Property, inverse z-transform, solution of difference equations, region of Convergence, bilinear (s to z) transform.

Module-III:
Walsh function and hadamard transform: generating walsh functions of Order n, characteristics and applications of walsh function, hadamard Matrix, properties, fast hadamard transform, applications

Module-IV:
Advanced Graph Theory: Connectivity, Matching, Hamiltonian Cycles, Coloring Problems, Algorithms for searching an element in a data structure (DFS, BFS).

Module-V:
A review of concepts of probability and random variables: Classical, relative frequency and axiomatic definitions of probability, addition rule, conditional probability, multiplication rule, Bayes' Theorem. Random Variables: Discrete and continuous random variables, probability mass, probability density and cumulative distribution functions, mathematical expectation, moments, moment generating function. Standard Distributions: Uniform, Binomial, Geometric, Negative Binomial, Poisson, Exponential, Gamma, Normal. Sampling Distributions: Chi-Square, t and F distributions. Estimation: The method of moments and the method of maximum likelihood estimation, confidence intervals for the mean(s) and variance(s) of normal populations. Testing of Hypotheses: Null and alternative hypotheses, the critical and acceptance regions, two types of error, power of the test, the most powerful test, tests of hypotheses on a single sample, two samples.

Reference Books:

1) N. Deo, Graph Theory with Applications to Engineering and Computer Science.
2) Dimitris G. Manolakis and John G Proakis, Digital Signal Processing: Principles, Algorithms, and Applications.
3) Alexander M. Mood, Franklin A. Graybill and Duane C. Boes, Introduction to the Theory of Statistics, 3rd Ed., Tata McGraw- Hill, Reprint 2007.
4) Sheldon Ross, Introduction to Probability Models, 9th Ed., Academic Press, Indian Reprint, 2007.
5) A. D. Poularikas, The Transforms and Applications Handbook, CRC Press, 1996.

Course Outcomes: At the end of the course, students will be able to:

CO 1: Characterize and represent data collected from experiments using statistical methods.
CO 2: Solve Boundary value and Initial value problems.
CO 3: To formulate problems in graph theoretic terms such as using graph coloring and matching theory.
CO 4: Apply statistical theories to solve engineering problems.
CO 5: Provide advanced knowledge on topics in pure mathematics, empowering the students to pursue higher degrees at reputed academic institutions.

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CO-PO Mapping

Subject	Course Outcomes	POs			
		1	**2**	**3**	**4**
Advanced Engineering Mathematics	1. Characterize and represent data collected from experiments using statistical methods.	1	1	1	1
	2. Model physical process/systems with multiple variables towards parameter estimation and prediction.	2	1	2	2
	3. Represent systems/architectures using graphs and trees towards optimizing desired objective.	1	1	1	1
	4.Provide knowledge of a wide range of mathematical techniques and application of mathematical methods/tools in other scientific and engineering domains.	2	2	2	1
	5.Provide advanced knowledge on topics in pure mathematic to pursue higher degrees at reputed academic institutions.	2	2	2	2
Note: '3' in the box for '**high-level'mapping**, 2 for '**Medium-level'mapping**, 1 for '**Low-level' mapping**.					

PGMVD206: Audit II : English for Research Paper Writing
[Sem – II] (L:2; T:0; P:0) (25 Lectures) CREDIT-0

Course objectives:

Students will be able to:

- Understand that how to improve your writing skills and level of readability
- Learn about what to write in each section
- Understand the skills needed when writing a Title Ensure the good quality of paper at very first-time submission

Syllabus:

Same as PGMVD-106 : Audit I : English for Research Paper Writing

PGMVD206: Audit II : Disaster Management [Sem – II]
(L:2; T:0; P:0) (25 Lectures) CREDIT-0

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Course Objectives:

Students will be able to:

1. learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
2. critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
3. develop an understanding of standards of humanitarian response and pract ical relevance in specific types of disasters and conflict situations. critically understand the strengths and weaknesses of disaster management approaches, planning andprogramming in different countries, particularly their home country or the countriesthey workin

Syllabus:

Same as PGMVD-106 : Audit I : Disaster Management

PGMVD206: Audit II : Sanskrit for Technical Knowledge [Sem – II] (L:2; T:0; P:0) (25 Lectures) CREDIT-0

CourseObjectives:

1. To get a working knowledge in illustrious Sanskrit, the scientific languagein the world
2. Learning of Sanskrit to improve brainfunctioning
3. Learning of Sanskrit to develop the logic in mathematics, science &other subjects enhancing the memorypower
4. The engineering scholars equipped with Sanskrit will be able to explore the hugeknowledge from ancientliterature

Syllabus:

Same as PGMVD-106 : Audit I : Sanskrit for Technical Knowledge

Course Outcome:

Students will be able to

1. Understanding basic Sanskritlanguage
2. Ancient Sanskrit literature about science & technology can beunderstood
3. Being a logical language will help to develop logic instudents

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PGMVD206: Audit II : ValueEducation
[Sem – II] (L:2; T:0; P:0) (25 Lectures)CREDIT-0

CourseObjectives:

Students will be able to

1. Understand value of education and self-development
2. Imbibe good values instudents
3. Let the should know about the importance ofcharacter

Syllabus:

Same as PGMVD-106 : Audit I : Value Education

Course Outcome:

Students will be able to

1. Knowledge ofself-development
2. Learn the importance of Humanvalues
3. Developing the overallpersonality

PGMVD206: Audit II : Constitution of India [Sem – II]
(L:2; T:0; P:0) (25 Lectures) CREDIT-0

CourseObjectives:

Students will be able to:

l. Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
2. To address the growth of Indian opm10nregarding modern Indian intelle ctua l s'constitutiona l role and entitlem ent to civil and economic right s as well as theemergence of nationhood in the early years of Indian nationalism.
3. To address the role of socialism In India after the comm encement of the Bolshev ikRevolution in 1917 and its impact on the init ia l drafting of the Indian Constitution.

Syllabus:

Same as PGMVD-106 : Audit I : Constitution of India

Course Outcomes:

Students will be able to:

l.DiscussthegrowthofthedemandforcivilrightsinIndiaforthebulkofIndiansbeforethearrivalofGandhiinIndianpolitics.

2. Disc uss the intellectua lorigins of the framework of argument that inform edthe conceptualizationof socia l reforms leading to revolution inIndia.
3. Discuss the circumstances surrounding the foundation of the Congress SocialistParty [CSP] under the leadership of Jawaharlal Nehru and the eventual failure oftheproposalofdirectelectionsthroughadultsuffrageintheIndianConstitution.
4. DiscussthepassageoftheHinduCodeBillof1956.

PGMVD206: Audit II : Pedagogy Studies [Sem – II] (L:2; T:0; P:0) (25 Lectures) CREDIT-0

Maulana Abul Kalam Azad University of Technology, West Bengal

(Formerly West Bengal University of Technology)

Syllabus for M. Tech in Microelectronics and VLSI Technology(MVD)

(Applicable from the academic session 2023-2024)

CourseObjectives:

Students will be able to:

4. Review existing evidence on the review topic to inform programme design and policymakingundertakenbytheDfID,otheragenciesandresearchers.
5. Identify critica l evidence gaps to guide the development.

Syllabus:

Same as PGMVD-106 : Audit I : Pedagogy Studies

Course Outcomes:

Students will be able to understand:

1. What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries?
2. What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
3. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

PGMVD206: Audit II : Stress Management by Yoga [Sem – II]
(L:2; T:0; P:0) (25 Lectures) CREDIT-0

Course Objectives:

1. To achieve overall health of body and mind
2. To overcome stress

Syllabus:

Same as PGMVD-106 : Audit I : Stress Management by Yoga

Course Outcomes:

Students will be able to:

1. Develop healthy mind in a healthy body thus improving social health also
2. Improve efficiency

PGMVD206: Audit II : Personality Development through Life Enlightenment Skills [Sem – II] (L:2; T:0; P:0) (25 Lectures) CREDIT-0
Course Objectives: 1. To learn to achieve the highest goal happily 2. To become a person with stable mind, pleasing personality and determination 3. To awaken wisdom in students
Syllabus: Same as PGMVD-106 : Audit I : Personality Development through Life Enlightenment Skills
Course Outcomes: Students will be able to 1. Study of Shrimad-Bhagwad- Geeta will help the student in developing his personality and achieve the highest goal inlife 2. The person who has studied Geeta will lead the nation and mankind to peace and prosperity 3. Study of Neetishatakam will help in developing versatile personality ofstudents.

Department: Microelectronics and VLSI Technology **Year:** 1st **Course Name:** Microelectronics Lab-II **Credit:** 2	**Session:**2023-2024 **Semester:** II **Course Code:** PGMVD291 **Target Student:** PG **Contact:** (L:0; T:0; P:3)

Course Outcomes:
After completion of this course students are able to
CO1. Familiar about capacitance-voltage characteristics and electrical parameters of the device under test.
CO2. Understand about design and Simulation of the circuit using Multisim software.
CO3. Familiar about HMS3000 Hall Effect Measurement system and how to determination of p-type/n-type semiconductor using the system.
CO4. Understand the capacitance or inductance curve of DUT by varying the frequency.
CO5. Familiar about Surface treatment of silicon wafer.

1. Identify the three pins of the device under test. Draw the capacitance-voltage characteristics across the highly doped and least doped junctions. Extract barrier height, doping concentration,

and other parameters. Comment on it and conclude.

Measurement Condition:

a) Device under test: p-n junction Diode(IN4007)
b) Instrumental Frequency: 1Khz ,100KHz, 1MHZ
c) Modes of measurement :Cp-D, Cp-Rp, Cp-Q, Cp, OR Cs-D, Cs-Rs, Cs-Q, Cs
d) BIAS Voltage :0-5V (reverse bias)

2. Identify the components needed to build a low pass filter. Simulate the circuit using analysis program Multisim and build the circuit on NI ELVIS II board to find the output waveform . Comment on it and conclude.

3. Identify the device under test and draw its current-voltage Characteristics and state what electrical parametaers you can find out from the curve. Comment on it and conclude.

4.Identify the three pins of the device. Draw the current -voltage characteristics of the device and state what electrical parameters you can find out from the curve. Comment on it and conclude.

5. Surface treatment of silicon wafer by Annealing process.

6. Determination of p-type/n-type semiconductor and their characteristics using HMS3000 Hall Effect Measurement system.

7.Study on the capacitance or inductance curve of DUT by varrying the frequency up to 1MHz. Find the dissipation and the quality factor for the components. Comment on the curve to find its functionality?
Measurement Conditions: For DUT

Instrumental Frequency Range : 20Hz to 2MHz
Modes of measurement : Cp-D, Cp-Rp, Cp-Q, Cp or Cs-D, Cs-Rs, Cs-Q, Cs
Measurement Conditions: For DUT
Instrumental Frequency Range : 20Hz to 2MHz
Modes of measurement : Lp-D, Lp-Rp, Lp-Q, Lp or Ls-D, Ls-Rs, Ls-Q, Ls

9.Identify the device and its contacts. Draw the capacitance-voltage characteristics across the junction. Extract barrier height, doping concentration, and other parameters. Comment on it and conclude.
Measurement Conditions:

a) Device under test : p-n junction Diode(IN4007)
b) Instrumental Frequency : 1KHz, 100KHz, 1MHz
c) Modes of measurement : Cp-D, Cp-Rp, Cp-Q, Cp or Cs-D, Cs-Rs, Cs-Q, Cs
d) Bias Voltage : 0 to 5V (reverse bias)

CO-PO Mapping

Subject	Course Outcomes	Program Outcomes			
		1	2	3	4
Microelectronics Lab-II	CO1. Familiar about capacitance-voltage characteristics and electrical parameters of the device under test.	**2**	**1**	2	3
	CO2. Understand about design and Simulation of the circuit using Multisim software.	**2**	**1**	**2**	2
	CO3. Familiar about HMS3000 Hall Effect Measurement system and how to determination of p-type/n-type semiconductor using the system.	**2**	**1**	**2**	2
	CO4. Understand the capacitance or inductance curve of DUT by varying the frequency.	**1**	1	**2**	2
	CO5. Familiar about Surface treatment of silicon wafer.	2	1	2	3
Note: '3' in the box for '**high-level'mapping**, 2 for '**Medium-level'mapping**, 1 for '**Low-level' mapping**.					

Department: Microelectronics and VLSI Technology Year:1st Course Name: VLSI Design lab II Credit: 2	Session:2023-2024 Semester: II Course Code: PGMVD292 Target Student: PG Contact: **(L:0; T:0; P:3)**

Pre-requisites:
Student should have basic familiarity with analog circuit & VLSI design and should have knowledge about the **cadence virtuoso**.

Course Objective:
1. Student will be familiar about VLSI Tools like LT-Spice and cadence virtuoso for Schematic and Layout design.
2. Student will be able to design circuit on cadence virtuoso using the schematic editor window. They will be able to simulate circuit by launching ADE-L in the schematic editor window.
3. Student will be able to do transient, dc and ac analysis.
4. Student will be able to do circuit verification. The layout for the schematic has to be prepared using Layout-XL, and the same has to be physically verified.

COURSE OUTCOMEs(CO)

After completion of this course students are able to
CO1. Familiar about VLSI Tool like cadence virtuoso.
CO2. Design analog circuit using schematic editor window and also able to test the design.
CO3. Extract the Layout of analog circuits and CMOS circuits using Layout-XL.
CO4. Do transient, dc and ac analysis of the designed circuit using cadence virtuoso.
CO5. Understand the DRC check, LVS and RC Extraction, design circuits on LT-Spice Tool and able to test it, familiar about LT-Spice Tool.

List of Lab Assignments:

List of Lab assignments with LT-Spice and cadence virtuoso:

1. i) Familiar with VLSI Design Tools like: LT-Spice and cadence virtuoso, ii) Design the schematic of an Inverter using **cadence virtuoso** and verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

2. Design and simulate the schematic of the common source amplifier. And verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

3. Design and simulate the schematic of the common drain amplifier, and perform the physical verification for the layout of the same. Verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

4. Design and simulate the schematic of a stage differential amplifier and perform the physical verification for the layout of the same. Verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

5. Design and simulate the schematic of the operational amplifier and perform the physical verification. Verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

6. Design and simulate the schematic of the of cascade current mirror and perform the physical verification. Verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

7. Design and simulate the schematic of wilson current mirror and perform the physical verification. Verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

CO-PO Mapping

Subject	Course Outcomes	Program Outcomes

		1	2	3	4
VLSI Design Lab-II	CO1. Familiar about VLSI Tool like cadence virtuoso.	2	2	3	2
	CO2. Design analog circuit using schematic editor window and also able to test the design.	1	2	3	2
	CO3. Extract the Layout of analog circuits and CMOS circuits using Layout-XL.	1	2	2	2
	CO4. Do transient, dc and ac analysis of the designed circuit using cadence virtuoso.	1	2	2	3
	CO5. Understand the DRC check, LVS and RC Extraction, design circuits on LT-Spice Tool and able to test it, familiar about LT-Spice Tool.	1	2	3	3
Note: '3' in the box for '**high-level mapping**, 2 for '**Medium-level mapping**, 1 for '**Low-level' mapping**.					

SEMESTER – III

Department: Microelectronics and VLSI Technology **Year:** 1st **Course Name:** Algorithms **Credit:** 3	**Session:**2023-2024 **Semester:** III **Course Code:** PGMVD301A **Target Student:** PG **Contact:** **(L:3; T:0; P:0)**

Prerequisite*: Concept of Programming, mathematical concepts such as Logarithms, Graph Theory.*

Course content:

Module 1: Introduction to Algorithms (7): Concept of Algorithm, The Role of an Algorithm in Computing, Fundamentals of Algorithm, Important Types of Algorithm, Introduction Analysis Framework, Methodologies for Analyzing Algorithms, Amortization, and Case Studies in Algorithm Analysis. Asymptotic Notations, Mathematical Analysis of Non-recursive and Recursive Algorithms, Graph theoretical Algorithms: Graph search Algorithms, Spanning tree Algorithm, Shortest path Algorithm, Matching Algorithm, Min cut and Max cut Algorithms and Steiner Tree Algorithm. Introduction to Scripting Language like Perl/ Python.

Module 2: NP-Complete Problem (8): NP-class of problems, P-class problems, NP=P question, Polynomial problem reduction (Reducibility), Cook's theorem, NP-hardness and NP-completeness, Examples of NP-completeness proofs: SAT to 3-SAT, Polynomial-time non-deterministic algorithms, Maximum Clique Problem.

Module 3: High-Level Synthesis (8): Steps of VLSI Design flow, Steps of High-Level Synthesis. Data Dependency graph. Scheduling Algorithms, Allocation, and Binding: Conflict Graph, Compatibility Graph, left Edge Algorithm, Data Path, and Controller Synthesis. Secure Design with HLS: different methods of obfuscation. Logic level Synthesis. Line sweep method. Graph Algorithms for Physical Design: Classes of graphs in physical design, the relationship between graph classes, graph problems, and Algorithms for interval graphs.

Module 4: Partitioning (2): Group migration Algorithms. Floor planning and Pin assignment: Slicing, Non-Slicing.

Module 5: Placement (2): Simulated annealing, simulated evolutions, force-directed placement, sequence pair technique.

Module 6: Routing (6): Routing Algorithms. Shortest path algorithm, Steiner tree-based Algorithm. Single-layer Routing Algorithms and two-layer Routing Algorithms. Over-the-cell routing Via minimization, clock, power, and ground routing. Topological Sort.

Module 7: Advanced Algorithms (7): Machine Learning Algorithms: Supervised, Unsupervised and Reinforcement Learning, Heuristic Algorithms: Hill Climbing, Best-first Search, Genetic Algorithms, Concept of ANN, Applications of CNN.

Suggested books

1. Naveed Sherwani, “Algorithms for VLSI Physical Design Automation” 3rd edition, Springer International, 1998.
2. Pinaki Mazumber, Elizabeth M Rudnick, “Genetic Algorithms For VLSI Design, Layout & Test Automation”, Pearson Education, 2007.
3. Ellis Horowitz, Sartaj Sahni, Sanguthevar Rajasekaran, “Fundamentals of Computer Algorithms” Universities Press.
4. Thomas H Cormen, Charles E Lieserson, Ronald L Rivest and Clifford Stein, “Introduction to Algorithms”, 4TH Edition, MIT Press/McGraw-Hill.
5. S.N. Sivanandam, S. N. Deepa, "Principles of Soft Computing", 2nd Edition, Wiley.

Suggested references

1. Jon Kleinberg and ÉvaTardos, “Algorithm Design”, 1ST Edition, Pearson.
2. Michael T. Goodrich and Roberto Tamassia, “Algorithm Design: Foundations, Analysis, and Internet Examples”, Second Edition, Wiley.
3. Udi Manber, Addison-Wesley, “Algorithms -- A Creative Approach”, 3RD Edition, Addison-Wesley Publishing Company.
4. “C-Based VLSI Design” lecture note of prof. Chandan Karfa, IIT Guwahati.

COURSE OUTCOMES(CO)

After completion of this course students are able to

CO1. Understand Different aspects of Algorithms: Complexity, Notations, and Analysis.

CO2. Understand and apply graph minimization algorithms on VLSI net-lists in Structural Design.
CO3. Determine the concept over NP class problems.
CO4. Understand and write code for partitioning, floor planning, chip planning, pin assignment, Placement and Routing during the physical design of a chip.
CO5. Apply optimization algorithms in various aspects of VLSI Design steps including Hardware Security.

CO-PO Mapping

CO	BL	Course Outcomes	Program Outcomes			
			1	**2**	**3**	**4**
1.	2	Understand Different aspects of Algorithms: Complexity, Notations, and Analysis.	1	1	3	3
2.	2	Understand and apply graph minimization algorithms on VLSI net-lists in Structural Design.	2	1	3	3
3.	2	Determine the concept over NP class problems.	2	1	3	3
4.	3	Understand and write code for partitioning, floor planning, chip planning, pin assignment, Placement and Routing during the physical design of a chip.	2	2	3	3
5.	3	Apply optimization algorithms in various aspects of VLSI Design steps including Hardware Security.	2	2	3	3
Note: '3' in the box for '**high-level ' mapping**, 2 for '**Medium-level mapping**, 1 for '**Low-level' mapping**.						

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